

Quicksilver_MLK Design

POWER

AC/BATT
CONNECTOR PG 57

BATT
CHARGER PG 50

CLK GEN

SLG8SP585

PG 5

SYSTEM POWER

SUS/ RUN POWER SW

+V5_SUS / +V5_RUN / +V1.5_RUN
+3.3V_ALW / +V3.3A_PCH / +V3.3_SUS / +V3.3_RUN

PG 58

CPU VR

+VCC_CORE

PG 51

VR

+V1.1S

PG 52

VR

+V1.1S_VTT

PG 53

REGULATOR For DDR3

+1.5V_DDR
+0.75V_DDR_VTT

PG 54

REGULATOR

+5V_ALW
+3.3V_ALW_17020

PG 55

LDO

+V1.8S

PG 56

Dual/Quad Core CPU
Intel
Arrandale / Clarksfield
(35W 2C/45W,55W 4C)
(989 rPGA)
37.5 x 37.5 mm

PG 6-12

DMI X 4

Intel
Ibex Peak M

(1071 Pin PBGA)
27 x 25 mm

PG 16-24

LPC

SM Bus

SPI

SPI

LPC

SPI

SPI

DDR III

DDR III

PCIEx8

PCIEx8

HDMI

DP-A

VGA

DP-D

Panel Connector

LVDS

DP-C

USB2.0

PCI-E

USB2.0

PCI-E

USB2.0

PCI-E

USB2.0

RGMII

Magnetic

RJ45

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DELL/FLEX CONFIDENTIAL

Title		
BLOCK DIAGRAM		
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Power States									
Power Rail	Control Signal	S0	S3	S4	S5	G3	S4/ M-off	S5/ M-off	
+PWR_SRC	N/A	V	V	V	V				
+0.75V_DDR_VTT	RUN_ON/SUS_ON	V	V						
+V1.1S_VTT	+V1.1S_VTT_MXM1_PWRON	V							
+V1.1S	RUN_ON	V							
+1.5V_RUN	RUN_ON#	V							
+1.5V_DDR	RUN_ON/SUS_ON	V	V						
+V1.8S	RUN_ON	V							
+3.3V_ALW	3VA_PCH_ON	V	V	V	V				
+3.3V_WLAN	AUX_EN_WOWL	V	define WOL	define WOL	define WOL				
+3.3V_RUN	RUN_ON#	V							
+V3.3	SUS_ON	V	V						
+5V_ALW	+5V_EN1/5V_ALW_ON	V	V	V	V				
+5V_ALW2	+PWR_SRC	V	V	V	V				
+5V_RUN	RUN_ON	V							
+5V_HDD	HDDC_EN	V							
+5V_MOD	MODC_EN	V							
+V5S	RUN_ON	V							
+LCDVCC	ENVDD	V							
+RTC_CELL	RTC	V	V	V	V	V			
+VCC_CORE	IMVP_VR_ON	V							
+USB_RIGHT_PWR	USB_SIDE_EN#	V	define	define					
+USB_LEFT_PWR	USB_BACK_EN#	V	define	define					
+15V_ALW	5V_ALW_ON	V	V	V	V				
+3.3V_ALW_17020	+3.3V_EN2/5V_ALW_ON	V	V	V	V				
+V3.3M_LAN	PM_SLP_LAN#	V	define WOL	define WOL	define WOL				

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Title		
FRONTPAGE		
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Clarksfield / Auburndale

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XDP port

SA_CK0
SA_CK1

SO-DIMM 1

SB_CK0
SB_CK1

SO-DIMM 2

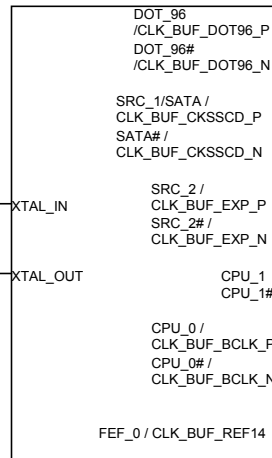
BCLK_ITP_P / BCLK_ITP
BCLK_ITP_N / BCLK_ITP#

CLK_EXP_P / PEG_CLK
CLK_EXP_N / PEG_CLK#

BCLK / BCLK_CPU_P
BCLK# / BCLK_CPU_N

IBex-Peak

ICS9LRS3191AKLFT CLK GEN



CLKOUT_PCIE0N / CLK_PCIE_EXPCARD#
CLKOUT_PCIE0P / CLK_PCIE_EXPCARD#

CLKOUT_PCIE1N / CLK_PCIE_MINI1#
CLKOUT_PCIE1P / CLK_PCIE_MINI1

CLKOUT_PCIE2N / CLK_PCIE_MINI2#
CLKOUT_PCIE2P / CLK_PCIE_MINI2

CLKOUT_PCIE3N / CLK_PCIE_MINI3#
CLKOUT_PCIE3P / CLK_PCIE_MINI3

CLKOUT_PCIE4N / CLK_PCH_SRC4_N
CLKOUT_PCIE4P / CLK_PCH_SRC4_P

CLKOUT_PCIE5N / NC_CLK_PCH_SRC5_N
CLKOUT_PCIE5P / NC_CLK_PCH_SRC5_P

CLKOUT_PEG_A_N / CLK_PCIE_VGA1#
CLKOUT_PEG_A_P / CLK_PCIE_VGA1

CLKOUT_PEG_B_N / CLK_PCIE_VGA2#
CLKOUT_PEG_B_P / CLK_PCIE_VGA2

SML0CLK / SML0_CLK
SML0DATA / SML0_DATA

SML1CLK / SMBCLK2
SML1DATA / SMBCLK2

CLKOUT_PCIE10 / CLK_PCH_PCCARD#

CLKOUT_PCIE11 / CLK_PCH_FB#
CLKIN_PCH_LOOPBACK / CLK_PCH_FB

JTAG_TCK / PCH_XDP_TCLK

CLKOUT_PCIE12 / CLK_LPC
CLKOUT_PCIE12 / CLK_LPC_DEBUG

CLKOUT_PCIE13

MXM-III 3.0 1

MXM-III 3.0 2

Debug Port

Hanksville

KBC

Card Reader(5C833)

Flash Cache
Module LPC

BT, UWB
Connector

EXPRESS
Card
connector

MiniCard
WLAN
Connector

Flash
Cache
Module
BT, UWB
Connector

MiniCard
WWAN
Connector

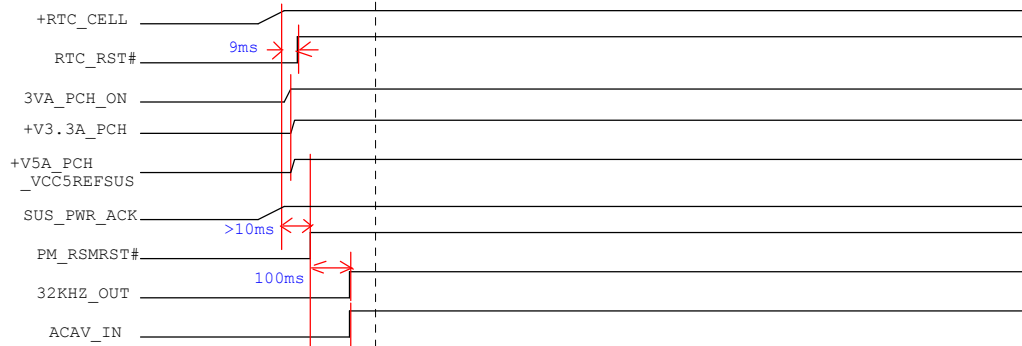
PHY GbE LAN

25MHz

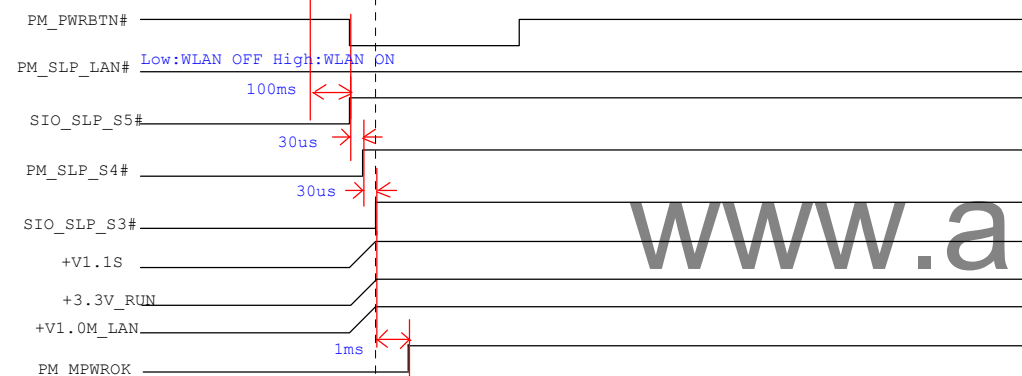
24.576MHz

Title			
CLOCK MAP			
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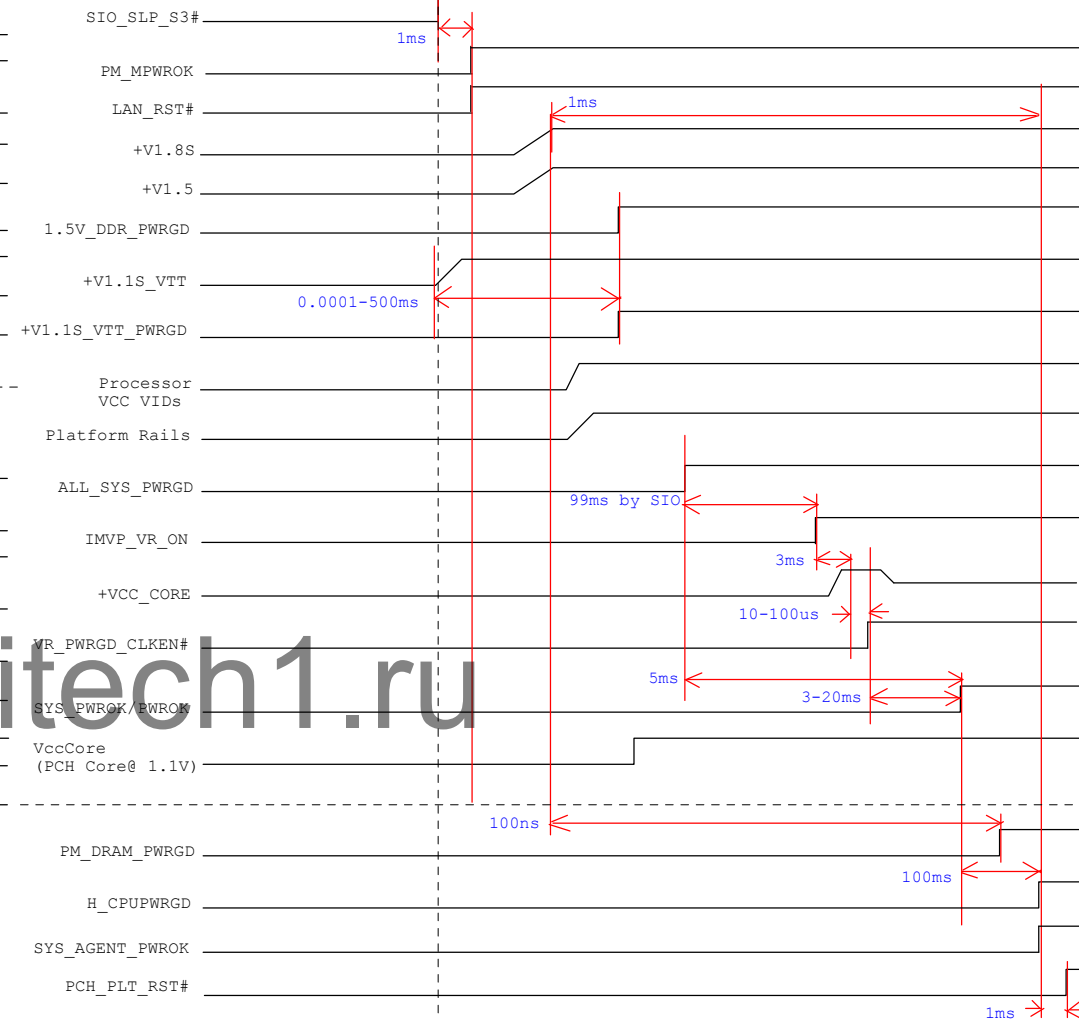
G3 to Sx



Sx to S0



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Title		
POWER SEQUENCING		
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IDT Clock gen	L16	R88	C139	R114
9LRS3191	NA	Add	NA	Add
9LRS3185	Add	NA	Add	NA

	Vender	Vender P/N	FLEX P/N
MAIN	IDT	ICS9LVS3185yKLFT	DELH-12D00J00000006G

VDD_I/O can be ranging from 1.05V to 3.3V.

L18
BLM18AG121SN1D
L0603

+V1.1S

+3.3V_RUN

L19
*BLM18AG121SN1D_NC
L0603

CLK_VCC: 40mil width
0.1uF near the every power pin.

IDD MAX 250mA

CLK_VCC_IO: 40mil width
0.1uF near the every power pin.

+1.5V_RUN

+3.3V_RUN

C164

33P/50V

C161

33P/50V

Y1
14.318MHz
20pF_+-30ppm

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

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33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

33P/50V

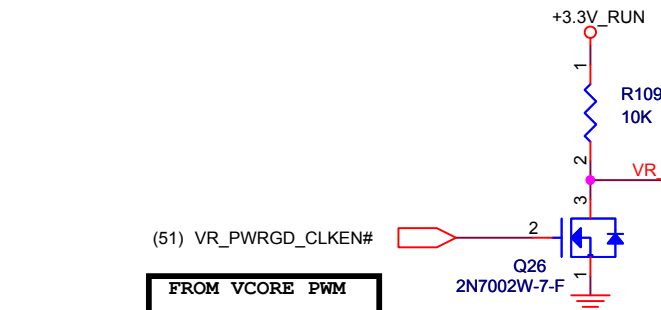
33P/50V

33P/50V

33P/50V

Number of Clock Outputs

Output	Number Output
133MHz	2
SRC(100MHz_SS)	1
SRC/SATA (100MHz)	1
REF (14.3181MHz)	1
DOT_CLK (96MHz)	1
27MHz	1
27MHz SS	1



(51) VR_PWRGD_CLKEN#

FROM VCORE PWM

www.tech1111.com

CLK BUF DOT96 P	C799	1	2	*10p/50V_NC
CLK BUF DOT96 N	C798	1	2	*10p/50V_NC
CLK BUF CKSSCD P	C180	1	2	*10p/50V_NC
CLK BUF CKSSCD N	C175	1	2	*10p/50V_NC
CLK BUF EXP P	C171	1	2	*10p/50V_NC
CLK BUF EXP N	C163	1	2	*10p/50V_NC
CLK BUF BCLK P	C134	1	2	*10p/50V_NC
CLK BUF BCLK N	C135	1	2	*10p/50V_NC
CLK BUF REF14	C194	1	2	*10p/50V_NC

EMI

Place all these 0 ohm resistors close to the CLK GEN

Mount for
ICS9LRS3191AKLFT

+3.3V_RUN

R114 *10K_NC

CPU_SEL During CK_PWRGD Latch Pin 30

Input (pin 30)	CPU_0/_1	SRC
0 -> NOW	133MHz	100MHz
1	100MHz	100MHz

R145 1 2 10K REF_0/CPU_SEL

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CLOCK GEN (SLG8SP585)		
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ARRANDALE /CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

U6A

(18) DMI_TXN0
(18) DMI_TXN1
(18) DMI_TXN2
(18) DMI_TXN3

(18) DMI_TXP0
(18) DMI_TXP1
(18) DMI_TXP2
(18) DMI_TXP3

(18) DMI_RXN0
(18) DMI_RXN1
(18) DMI_RXN2
(18) DMI_RXN3

(18) DMI_RXP0
(18) DMI_RXP1
(18) DMI_RXP2
(18) DMI_RXP3

A24 DMI_RX#[0]
C23 DMI_RX#[1]
B22 DMI_RX#[2]
A21 DMI_RX#[3]

B24 DMI_RX#[0]
D23 DMI_RX#[1]
B23 DMI_RX#[2]
A22 DMI_RX#[3]

D24 DMI_TX#[0]
G24 DMI_TX#[1]
F23 DMI_TX#[2]
H23 DMI_TX#[3]

D25 DMI_TX#[0]
F24 DMI_TX#[1]
E23 DMI_TX#[2]
G23 DMI_TX#[3]

T670 PAD FDI_TXN0

E22 FDI_TX#[0]
D21 FDI_TX#[1]
D19 FDI_TX#[2]
D18 FDI_TX#[3]
G21 FDI_TX#[4]
E19 FDI_TX#[5]
F21 FDI_TX#[6]
G18 FDI_TX#[7]

T671 PAD FDI_TXP0

D22 FDI_TX#[0]
C21 FDI_TX#[1]
D20 FDI_TX#[2]
C18 FDI_TX#[3]
G22 FDI_TX#[4]
E20 FDI_TX#[5]
F20 FDI_TX#[6]
G19 FDI_TX#[7]

1K 2 1 R742 FDI_FSYNC0

1K 2 1 R742 FDI_FSYNC1

FDI_INT C17

FDI_LSYNC0 F18

FDI_LSYNC1 D17

1K 2 1 R744 FDI_INT

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

CLARKSFIELD CPU	FLEX P/N
Q820	DELH-11D0010000027G
X920	DELH-11D0010000026G

Arrandale CPU	FLEX P/N
520M	DELH-11D0010000037G

CPU_FOXCONN_PZ98927-3641-01F

DMI

PCI EXPRESS

PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO
PEG_RBIAS

PEG_RX#[0]
PEG_RX#[1]
PEG_RX#[2]
PEG_RX#[3]
PEG_RX#[4]
PEG_RX#[5]
PEG_RX#[6]
PEG_RX#[7]
PEG_RX#[8]
PEG_RX#[9]
PEG_RX#[10]
PEG_RX#[11]
PEG_RX#[12]
PEG_RX#[13]
PEG_RX#[14]
PEG_RX#[15]

PEG_RX#[0]
PEG_RX#[1]
PEG_RX#[2]
PEG_RX#[3]
PEG_RX#[4]
PEG_RX#[5]
PEG_RX#[6]
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PEG_RX#[8]
PEG_RX#[9]
PEG_RX#[10]
PEG_RX#[11]
PEG_RX#[12]
PEG_RX#[13]
PEG_RX#[14]
PEG_RX#[15]

PEG_TX#[0]
PEG_TX#[1]
PEG_TX#[2]
PEG_TX#[3]
PEG_TX#[4]
PEG_TX#[5]
PEG_TX#[6]
PEG_TX#[7]
PEG_TX#[8]
PEG_TX#[9]
PEG_TX#[10]
PEG_TX#[11]
PEG_TX#[12]
PEG_TX#[13]
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PEG_TX#[15]

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PEG_TX#[4]
PEG_TX#[5]
PEG_TX#[6]
PEG_TX#[7]
PEG_TX#[8]
PEG_TX#[9]
PEG_TX#[10]
PEG_TX#[11]
PEG_TX#[12]
PEG_TX#[13]
PEG_TX#[14]
PEG_TX#[15]

B26 PEG_IRCOMP R R91 1 2 49.9 F
A26 PEG_ICOMPO
B27 EXP_RBIAS R94 1 2 750 F

K35 PEG_RXN0
J34 PEG_RXN1
J33 PEG_RXN2
G35 PEG_RXN3
G32 PEG_RXN4
F34 PEG_RXN5
F31 PEG_RXN6
D35 PEG_RXN7
E33 PEG_RXN8
C33 PEG_RXN9
D32 PEG_RXN10
B32 PEG_RXN11
C31 PEG_RXN12
B28 PEG_RXN13
B30 PEG_RXN14
A31 PEG_RXN15

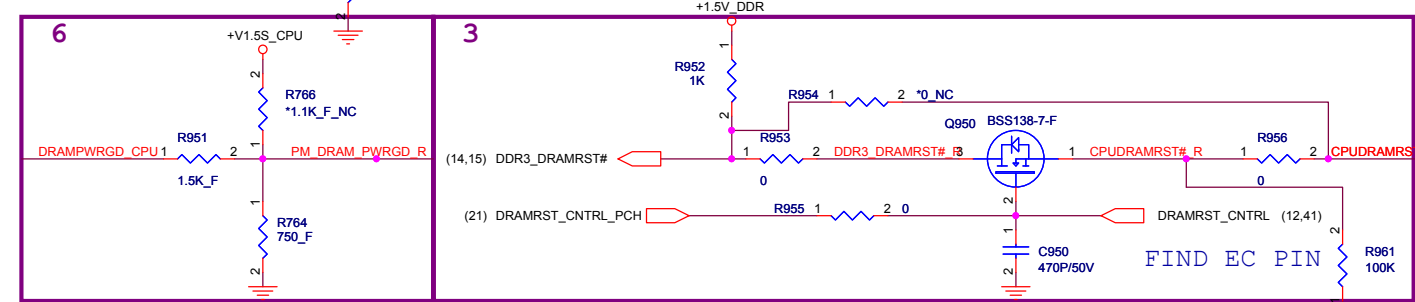
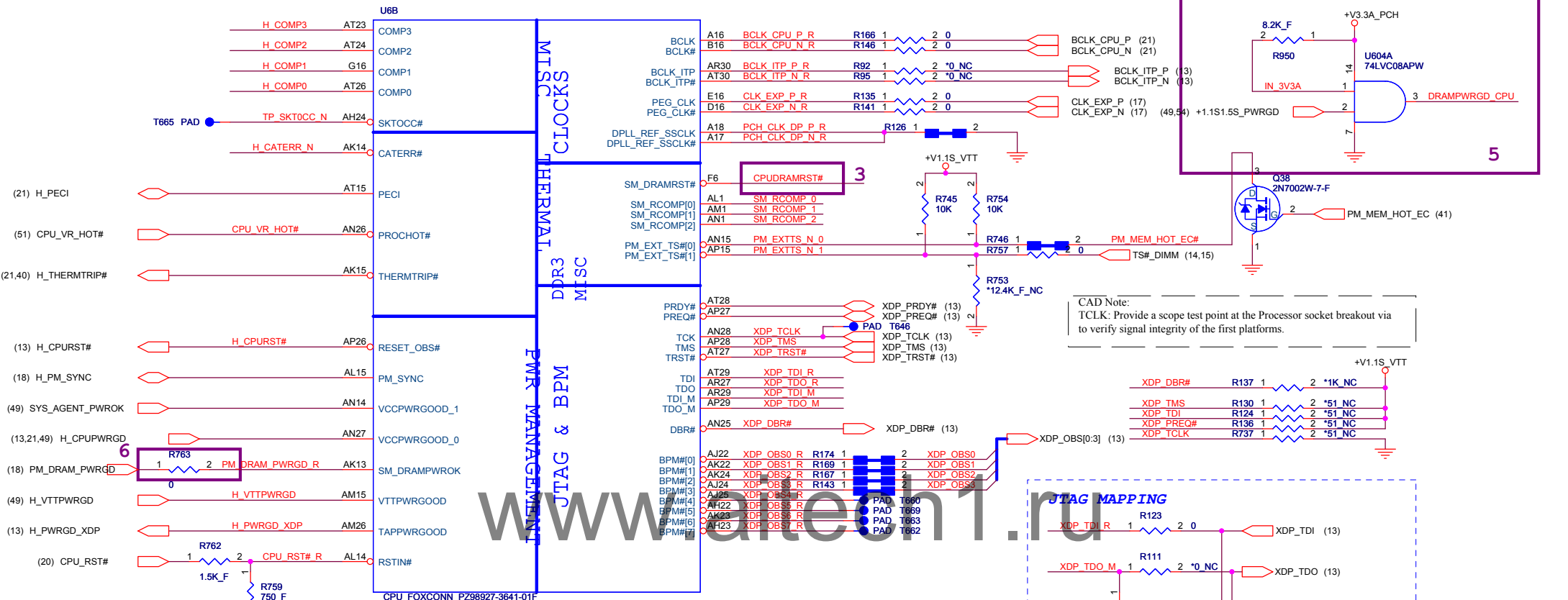
J35 PEG_RXP0
H34 PEG_RXP1
H33 PEG_RXP2
F35 PEG_RXP3
G33 PEG_RXP4
E34 PEG_RXP5
F32 PEG_RXP6
D34 PEG_RXP7
F33 PEG_RXP8
B33 PEG_RXP9
D31 PEG_RXP10
A32 PEG_RXP11
C30 PEG_RXP12
A28 PEG_RXP13
B29 PEG_RXP14
A30 PEG_RXP15

L33 PEG_C_TXN0
M35 PEG_C_TXN1
M33 PEG_C_TXN2
M30 PEG_C_TXN3
L31 PEG_C_TXN4
K32 PEG_C_TXN5
M29 PEG_C_TXN6
J31 PEG_C_TXN7
K29 PEG_C_TXN8
H30 PEG_C_TXN9
H29 PEG_C_TXN10
F29 PEG_C_TXN11
E28 PEG_C_TXN12
D29 PEG_C_TXN13
D27 PEG_C_TXN14
C26 PEG_C_TXN15

L34 PEG_C_TXP0
M34 PEG_C_TXP1
M32 PEG_C_TXP2
L30 PEG_C_TXP3
M31 PEG_C_TXP4
K31 PEG_C_TXP5
M28 PEG_C_TXP6
H31 PEG_C_TXP7
K28 PEG_C_TXP8
G30 PEG_C_TXP9
G29 PEG_C_TXP10
F28 PEG_C_TXP11
E27 PEG_C_TXP12
D28 PEG_C_TXP13
C27 PEG_C_TXP14
C25 PEG_C_TXP15

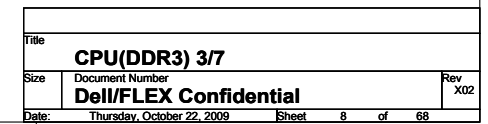
Title	
CPU (DMI,PEG,FDI) 1/7	
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Dell/FLEX Confidential	
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ARRANDALE /CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

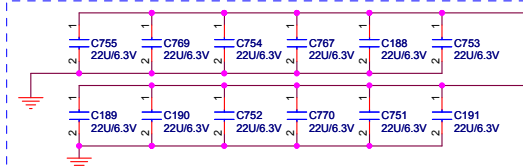


Scan Chain (Default)	
CPU Only	
GMCH Only	

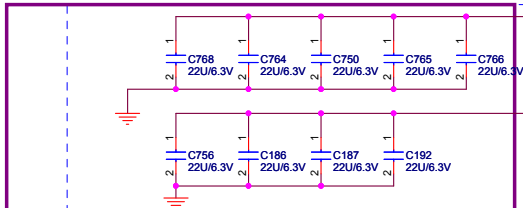
Diagram illustrating the mapping of System Memory A to M_A_DQS[7:0] (14). The diagram shows two columns of memory addresses. The left column lists SA_DQS#0 through SA_DQS#7, which are mapped to M_A_DQS#0 through M_A_DQS#7. The right column lists SA_DQS#8 through SA_DQS#15, which are mapped to M_B_DQS#0 through M_B_DQS#7. A red arrow points from the label M_A_DQS[7:0] (14) to the M_A_DQS#0 to M_A_DQS#7 mapping.



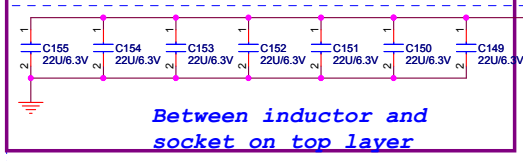
ARRANDALE /CLARKSFIELD PROCESSOR (POWER)



Under cavity of the socket



Place inside cavity of the socket



Between inductor and
socket on top layer

+VCC_CORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AD35 VCC20
AD34 VCC21
AD33 VCC22
AD32 VCC23
AD31 VCC24
AD30 VCC25
AD29 VCC26
AD28 VCC27
AD27 VCC28
AD26 VCC29
AC35 VCC30
AC34 VCC31
AC33 VCC32
AC32 VCC33
AC31 VCC34
AC30 VCC35
AC29 VCC36
AC28 VCC37
AC27 VCC38
AC26 VCC39
AA35 VCC40
AA34 VCC41
AA33 VCC42
AA32 VCC43
AA31 VCC44
AA30 VCC45
AA29 VCC46
AA28 VCC47
AA27 VCC48
AA26 VCC49
Y35 VCC50
Y34 VCC51
Y33 VCC52
Y32 VCC53
Y31 VCC54
Y30 VCC55
Y29 VCC56
Y28 VCC57
Y27 VCC58
Y26 VCC59
Y35 VCC60
Y34 VCC61
Y33 VCC62
Y32 VCC63
Y31 VCC64
Y30 VCC65
Y29 VCC66
Y28 VCC67
Y27 VCC68
Y26 VCC69
Y35 VCC70
Y34 VCC71
Y33 VCC72
Y32 VCC73
Y31 VCC74
Y30 VCC75
Y29 VCC76
Y28 VCC77
Y27 VCC78
Y26 VCC79
R55 VCC80
R34 VCC81
R33 VCC82
R32 VCC83
R31 VCC84
R30 VCC85
R29 VCC86
R28 VCC87
R27 VCC88
R26 VCC89
P35 VCC90
P34 VCC91
P33 VCC92
P32 VCC93
P31 VCC94
P30 VCC95
P29 VCC96
P28 VCC97
P27 VCC98
P26 VCC99
P25 VCC100

U6F

1.1V RAIL POWER

CPU CORE SUPPLY

POWER
CPU VIDS

SENSE LINES

+V1.1S_VTT

VTT0_1 AH14
VTT0_2 AH12
VTT0_3 AH11
VTT0_4 AH10
VTT0_5 J14
VTT0_6 J13
VTT0_7 H14
VTT0_8 H12
VTT0_9 G14
VTT0_9 G13
VTT0_10 G12
VTT0_11 G11
VTT0_12 F14
VTT0_13 F13
VTT0_14 F12
VTT0_15 F11
VTT0_16 E14
VTT0_17 E12
VTT0_18 D14
VTT0_19 D13
VTT0_20 D12
VTT0_21 D11
VTT0_22 C14
VTT0_23 C13
VTT0_24 C12
VTT0_25 C11
VTT0_26 B14
VTT0_27 B12
VTT0_28 B11
VTT0_29 A14
VTT0_30 A13
VTT0_31 A12
VTT0_32 A11

VTT0_33 AF10
VTT0_34 AE10
VTT0_35 AC10
VTT0_36 AB10
VTT0_37 Y10
VTT0_38 W10
VTT0_39 U10
VTT0_40 T10
VTT0_41 J11
VTT0_42 J10
VTT0_43 J16
VTT0_44 J15

Edge of the socket

EMI

Under cavity of the socket

+V1.1S_VTT33_VTT42

EMI

+V1.1S_VTT

+V1.1S_VTT

+V1.1S_VTT

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+V1.1S_VTT

+V1.1S_VTT

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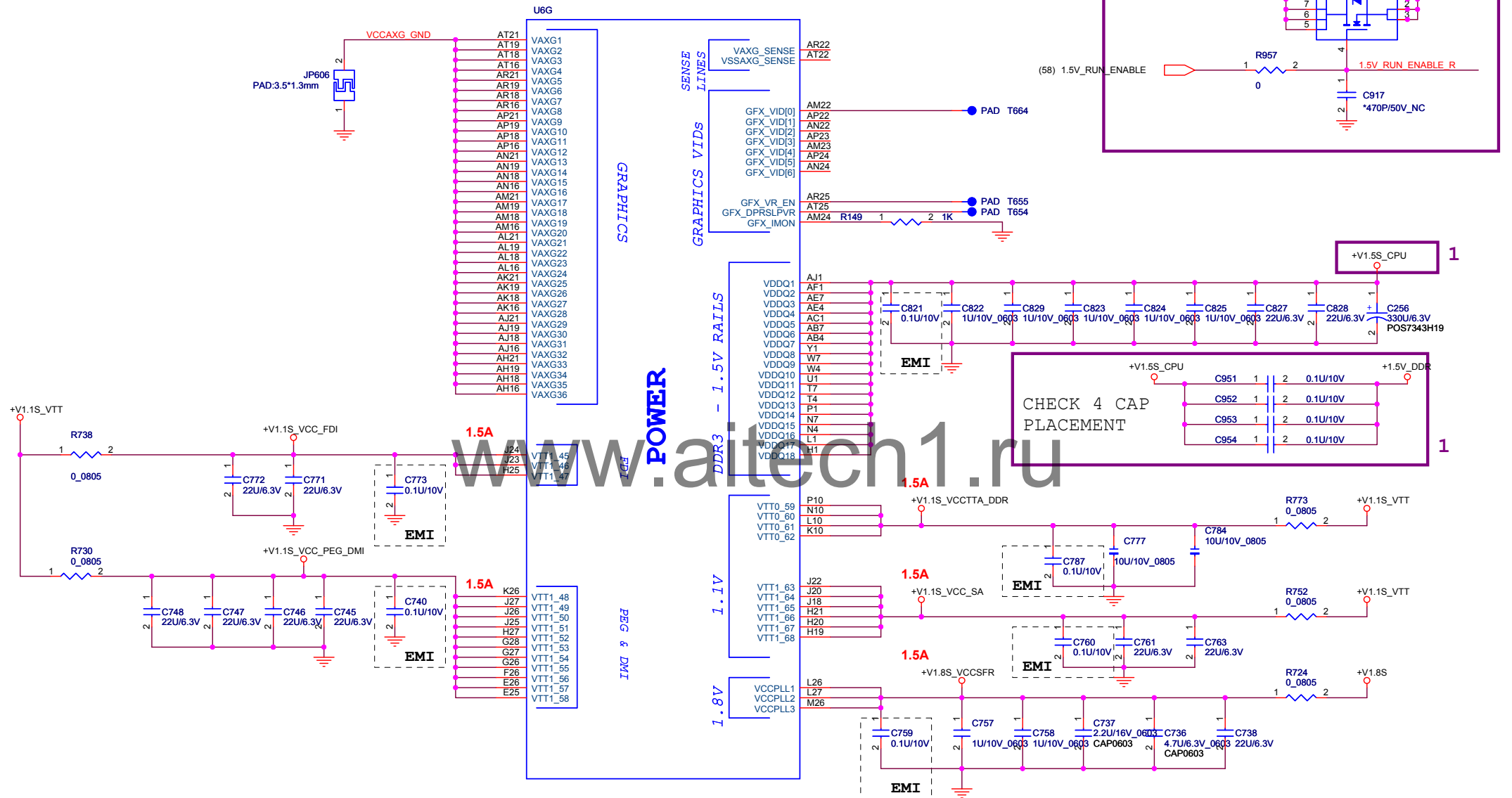
+V1.1S_VTT

+V1.1S_VTT

+V1.1S_VTT

+V1.1S_VTT

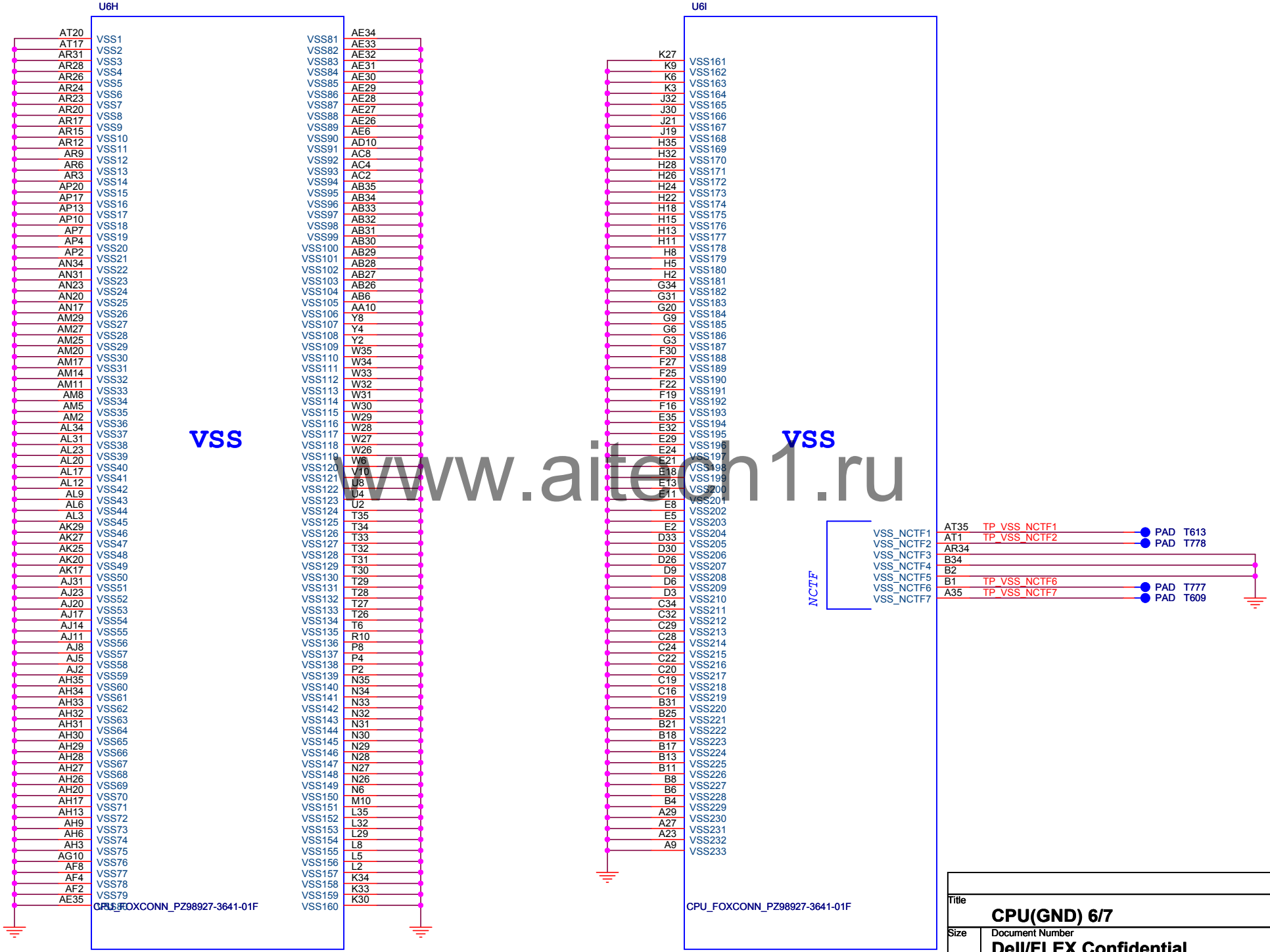
ARRANDALE /CLARKSFIELD PROCESSOR (GRAPHICS POWER)



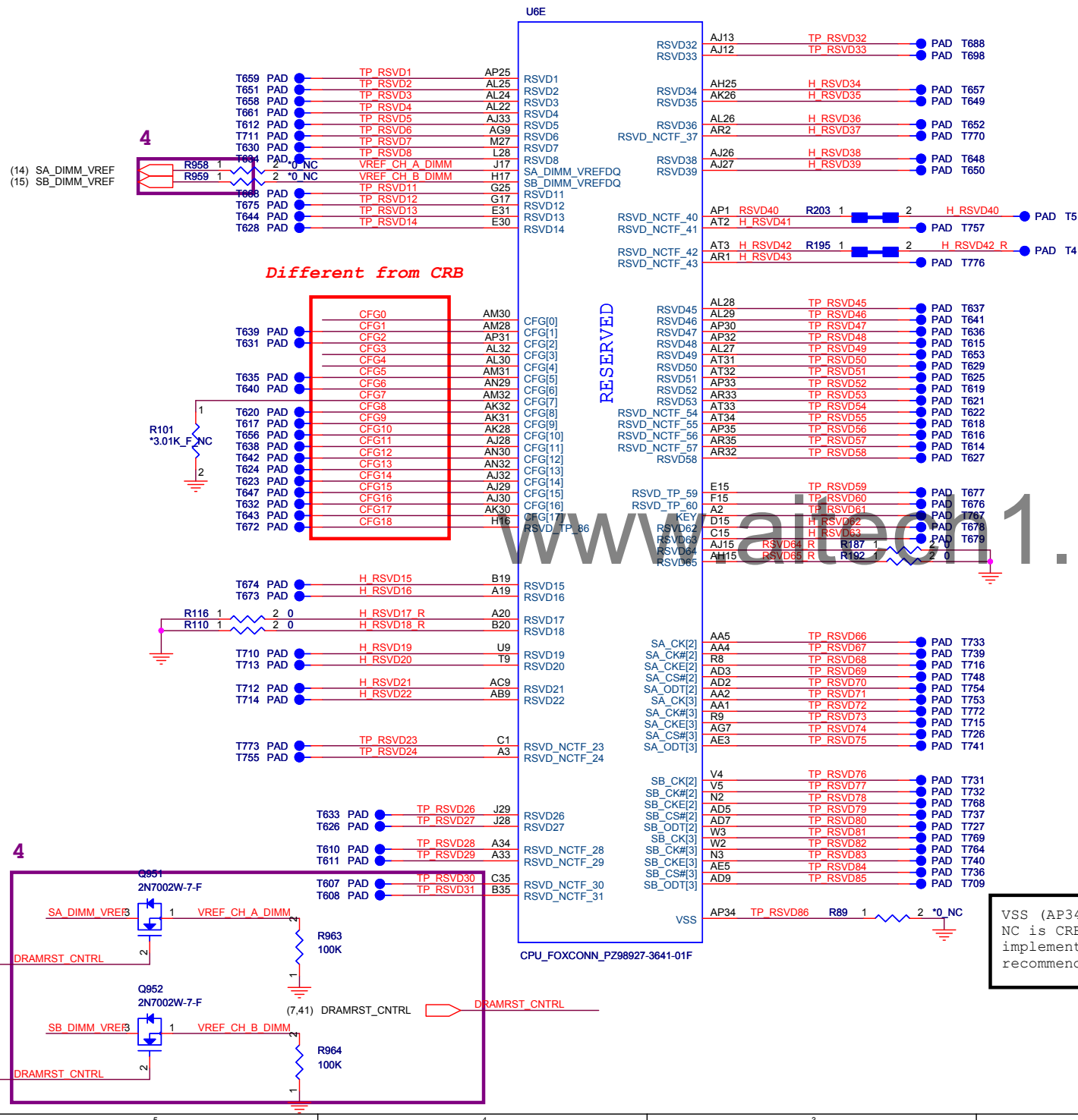
CPU_FOXCONN_PZ98927-3641-01F

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ARRANDALE /CLARKSFIELD PROCESSOR (GND)

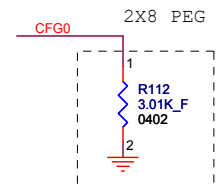


ARRANDALE /CLARKSFIELD PROCESSOR(RESERVED, CFG)

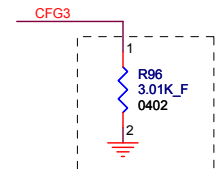


CFG Straps for PROCESSOR

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled



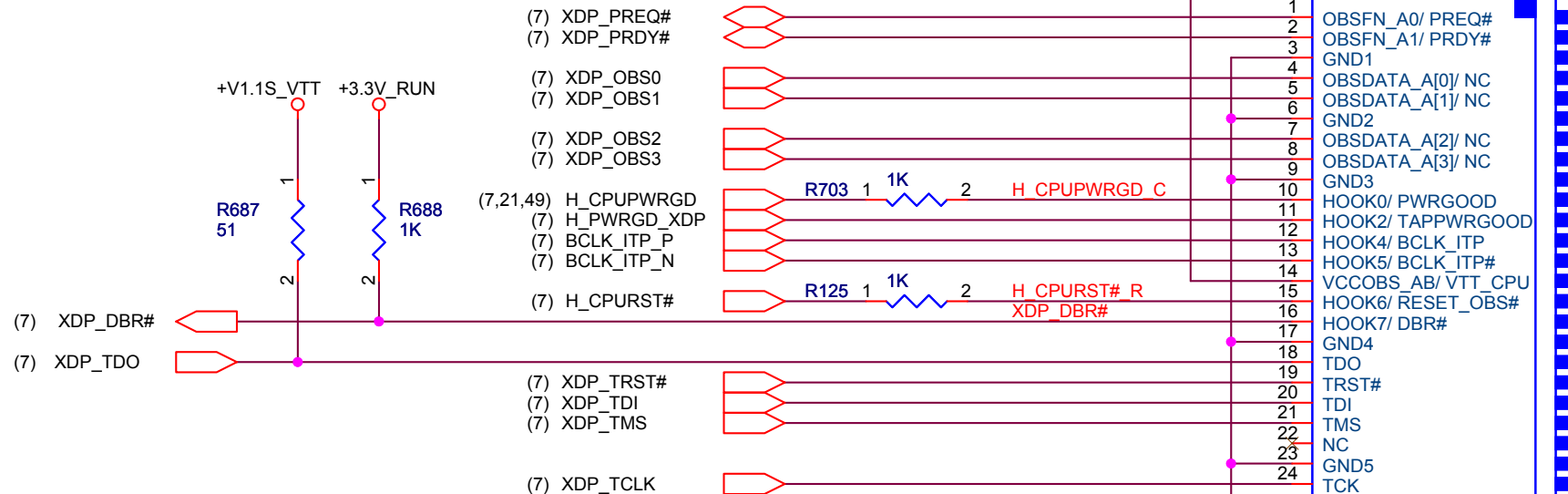
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation(Default) 0 : Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



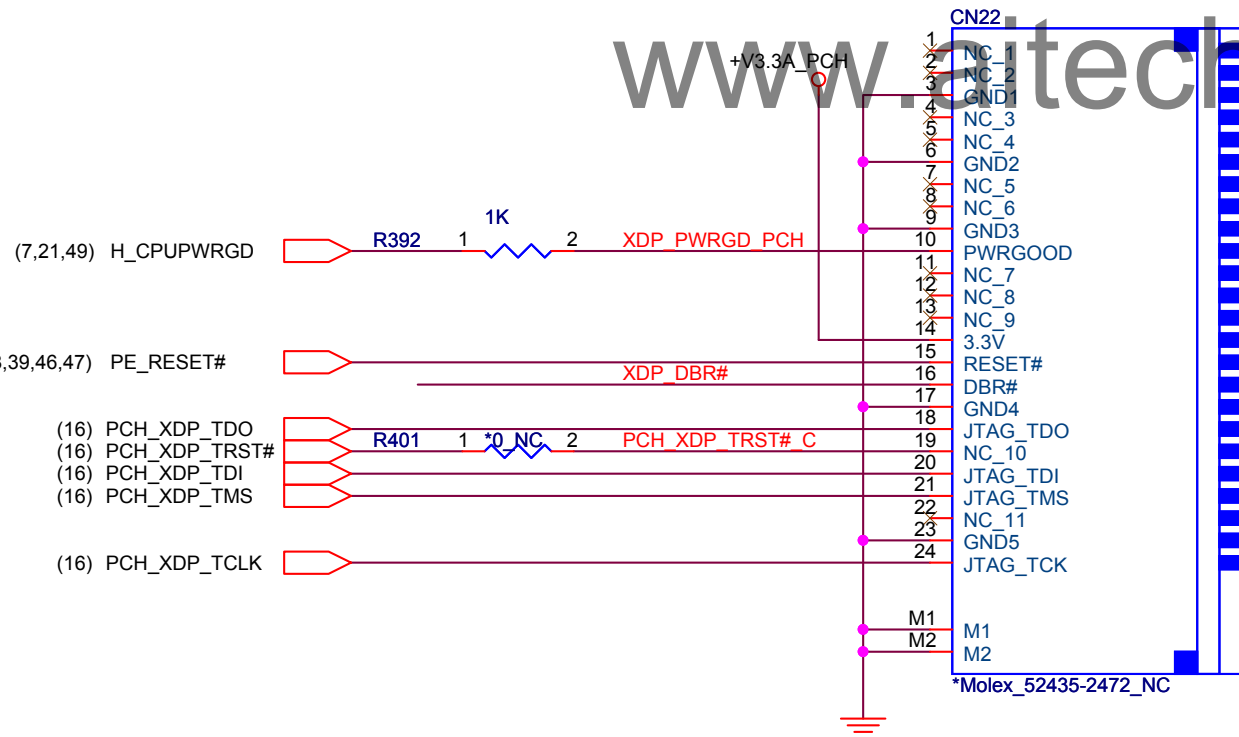
CFG4 - Display Port Presence	
CFG4	<p>1:Disabled; No Physical Display Port attached to Embedded Display Port (Default)</p> <p>0:Enabled; An external Display Port device is connected to the Embedded Display Port</p>



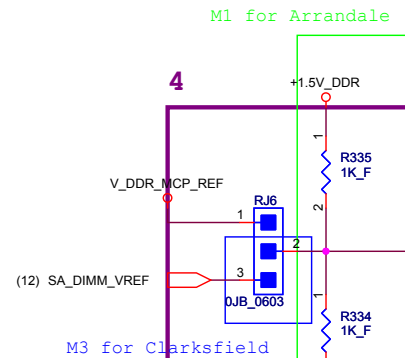
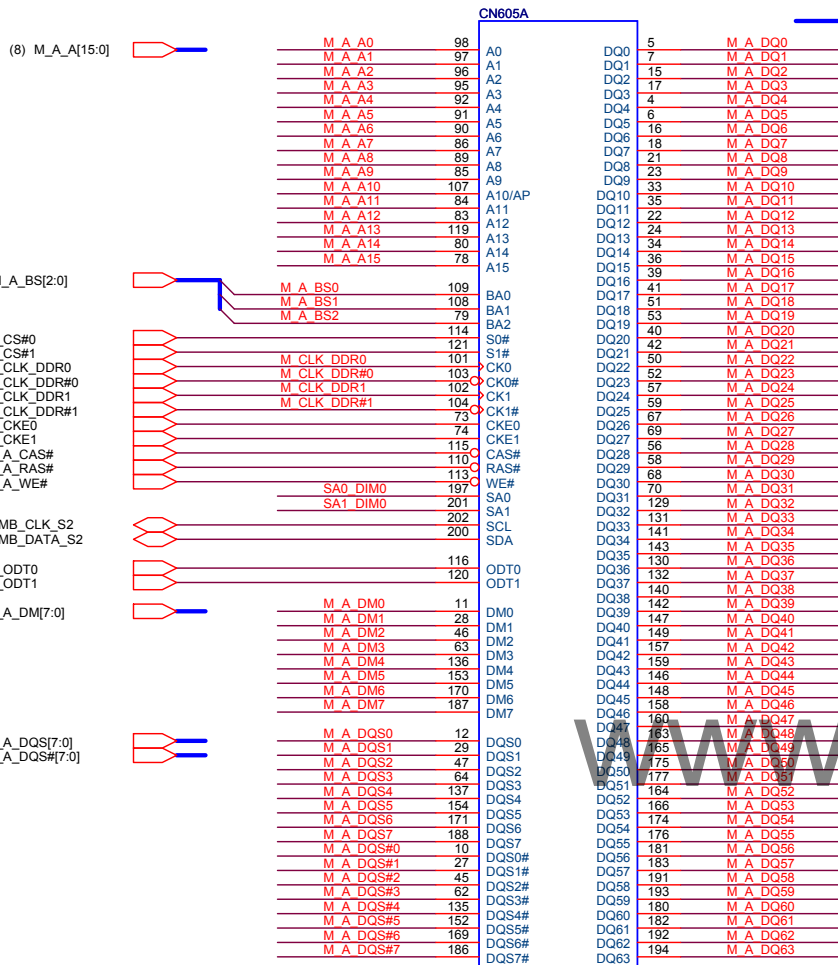
VSS (AP34) can be left
NC is CRB
implementation; EDS/DG
recommendation to GND



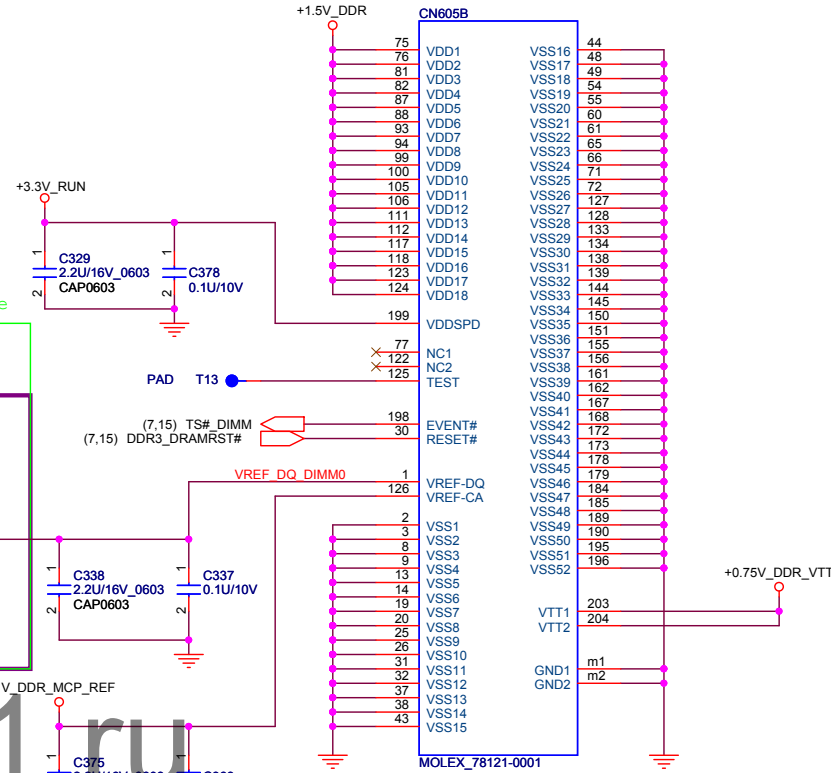
www.gitech1.ru



Title		
XDP(PROCESSOR / PCH)		
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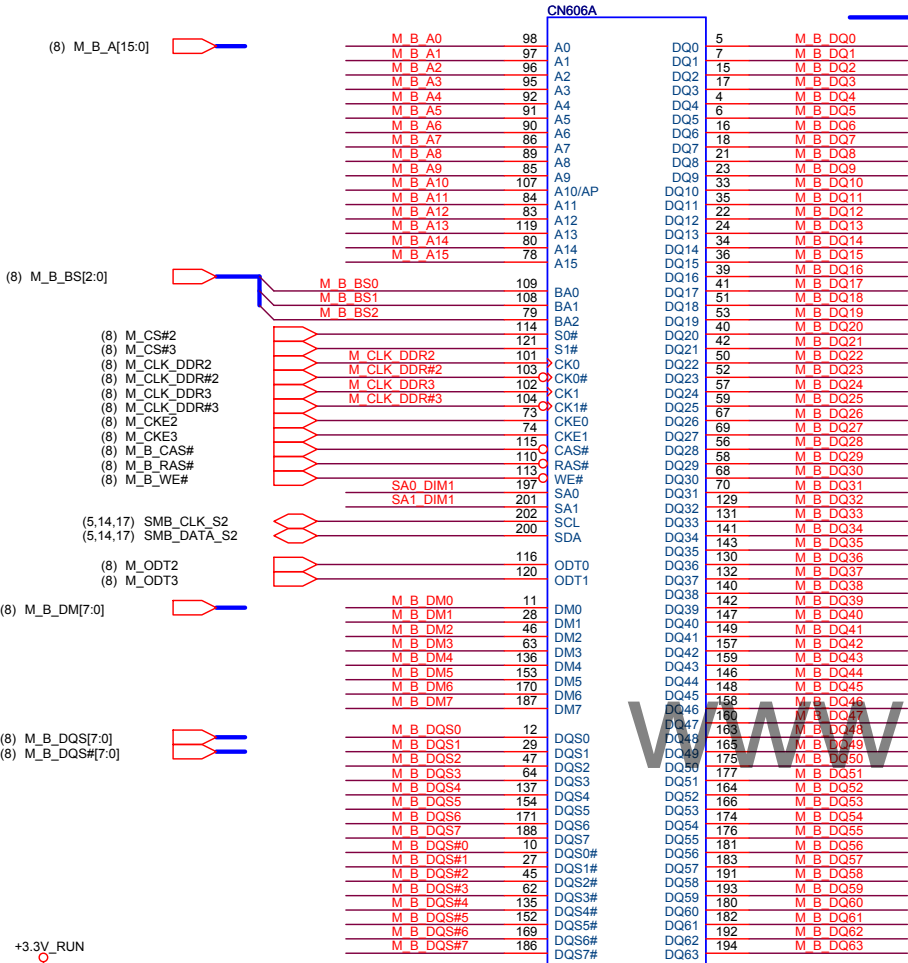
DESIGN 1.6 showed that both M1 and M3 should be concurrently implemented for both CPU



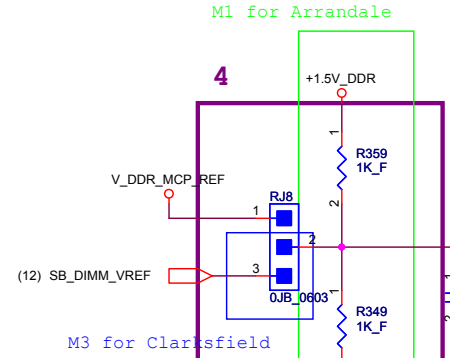
Place these caps close to Pin203 and 204.

Layout Note:
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin (9/9).

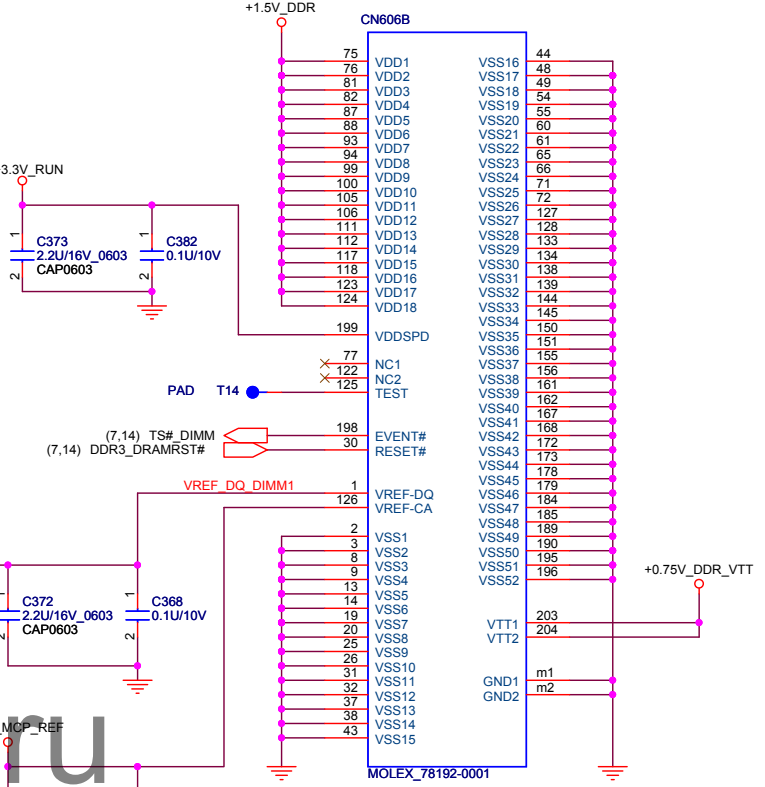
SO-DIMM Address		
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0
	TS	0x30
SA0_DIM0 = 1, SA1_DIM0 = 0	SPD	0xA2
	TS	0x32



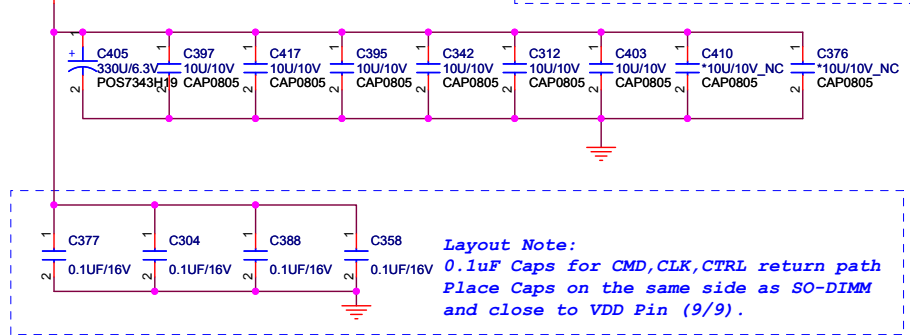
SO-DIMM Address	
SPD	0xA4
TS	0x34



DESIGN 1.6 showed that both M1 and M3 should be con-currently implemented for both CPU



SODIMM 2 DECOUPLING

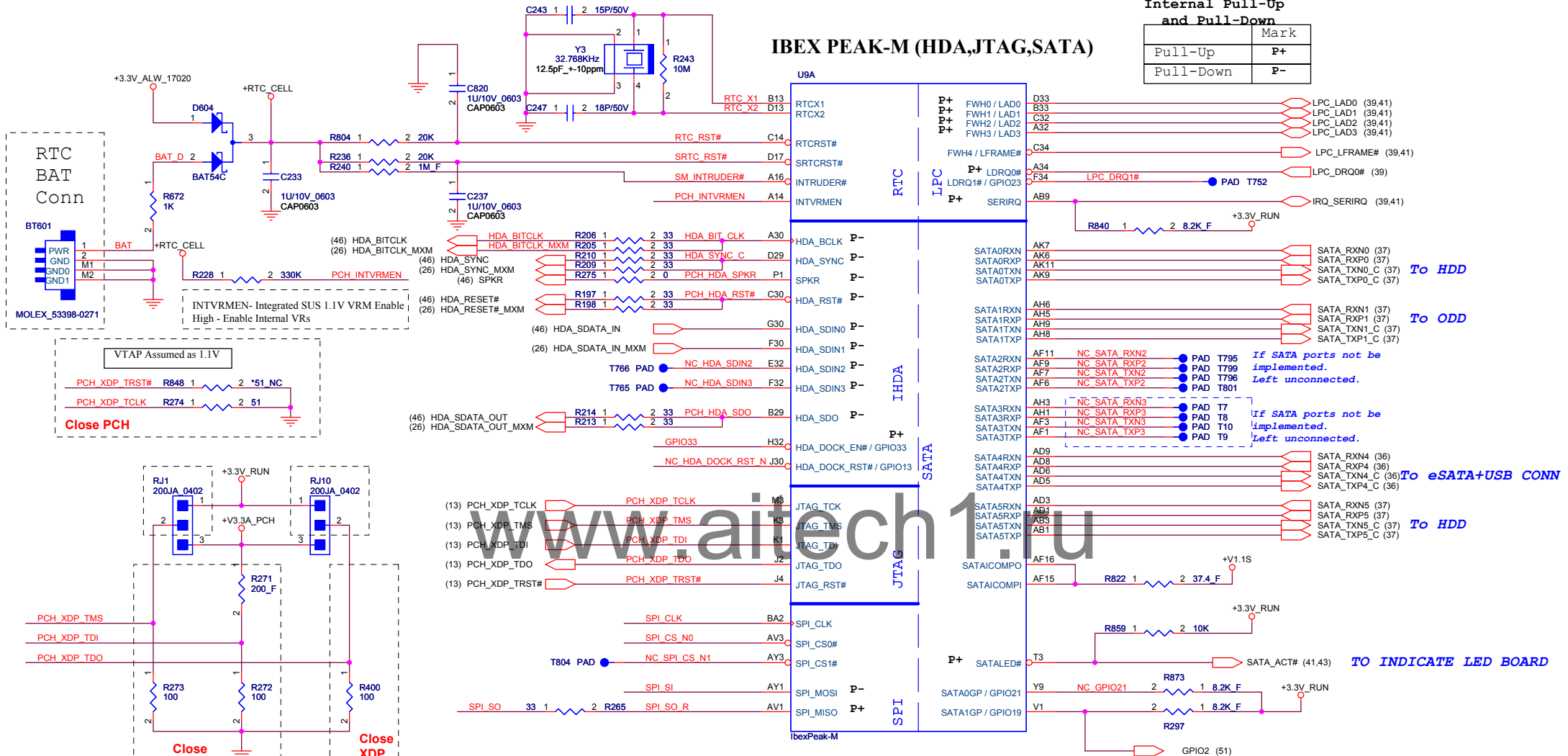


Layout Note:
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin (9/9).

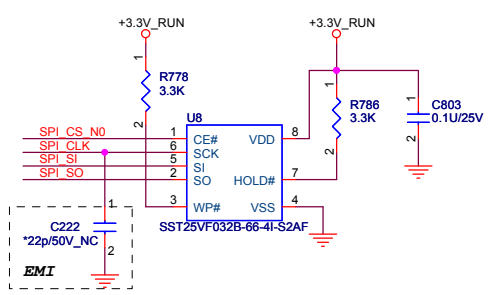
IBEX PEAK-M (HDA,JTAG,SATA)

Internal Pull-Up and Pull-Down

	Mark
Pull-Up	P+
Pull-Down	P-

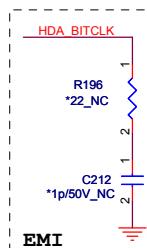


32Mbit (4M Byte) SPI, Support iME



NO REBOOT STRAP	
HDA_SPKR	NA Low=Default MOUNTED High=No Reboot

iTPM ENABLE/DISABLE	
SPI_SI	NA Low=Disable(Default) MOUNTED High=Enable

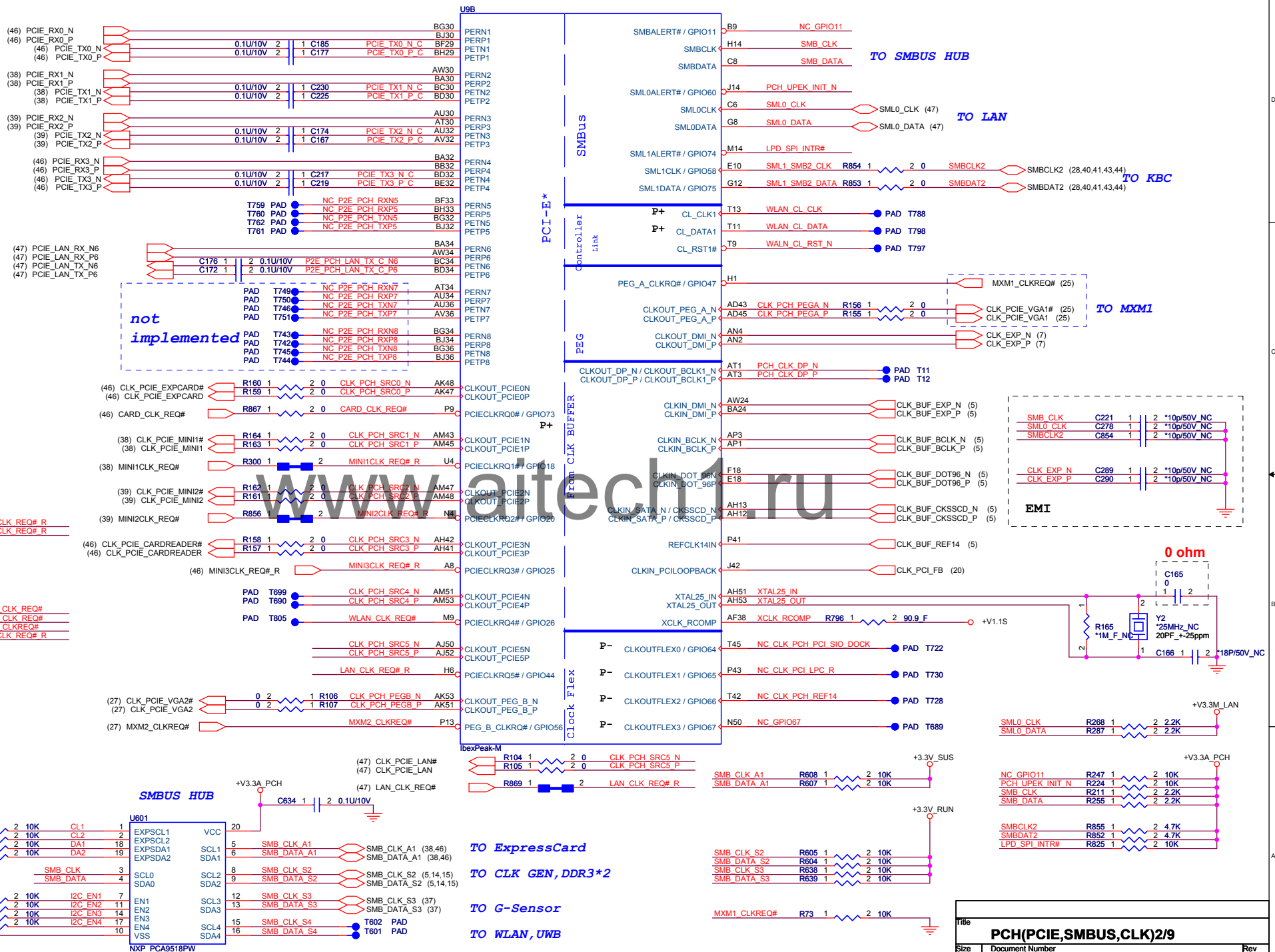


Flash Descriptor Security

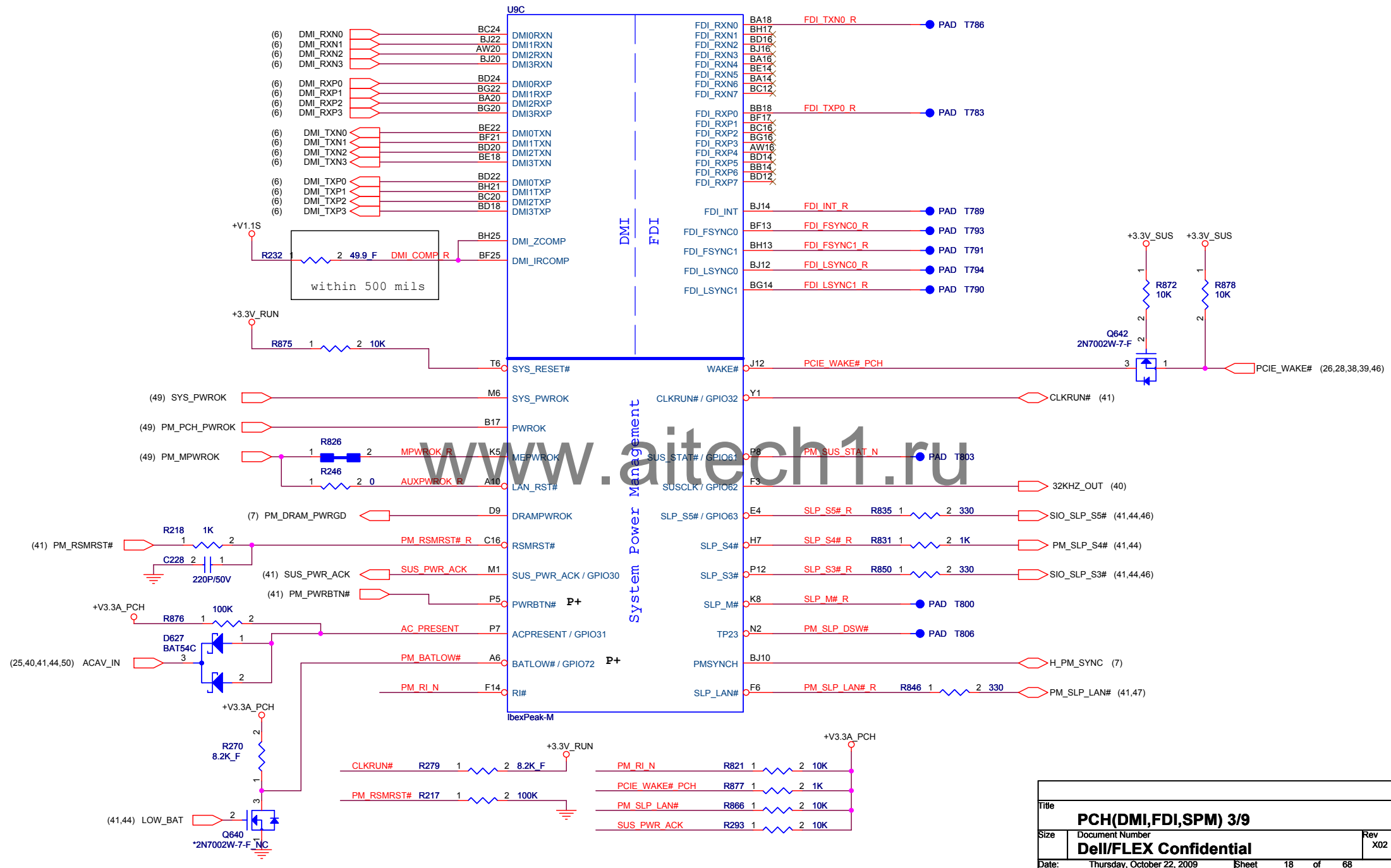
High	Flash Descriptor will be in effect (default)
Low	Descriptor Security will be overridden

IBEX PEAK-M (PCI-E,SMBUS,CLK)

PCI-E* x1	Usage
Lane 1	Express Card
Lane2	WiMax
Lane 3	BT
Lane 4	Card reader/1394
Lane 5	NC
Lane 6	PHY
Lane 7	NC
Lane 8	NC

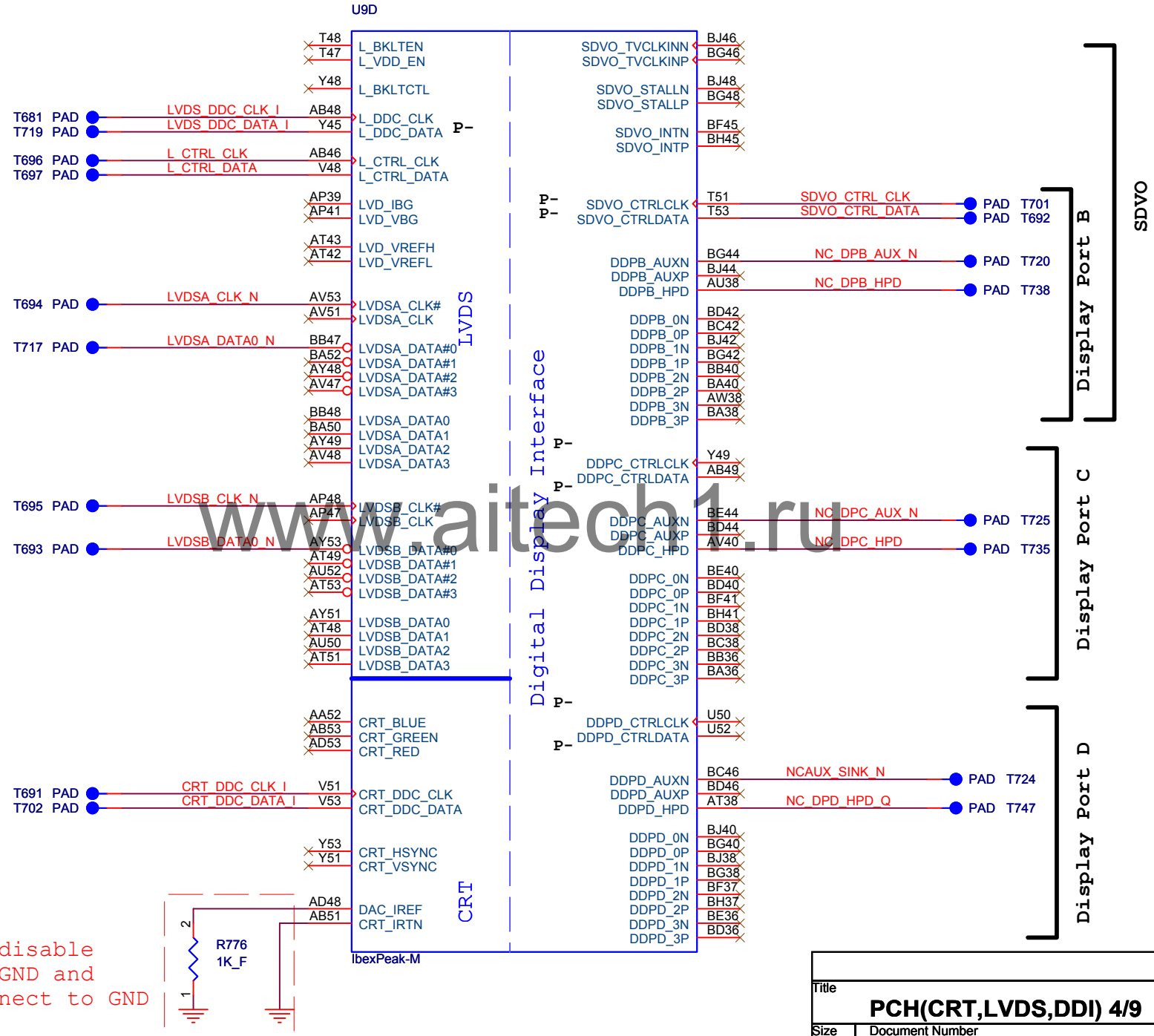


IBEX PEAK-M (DMI,FDI,GPIO)

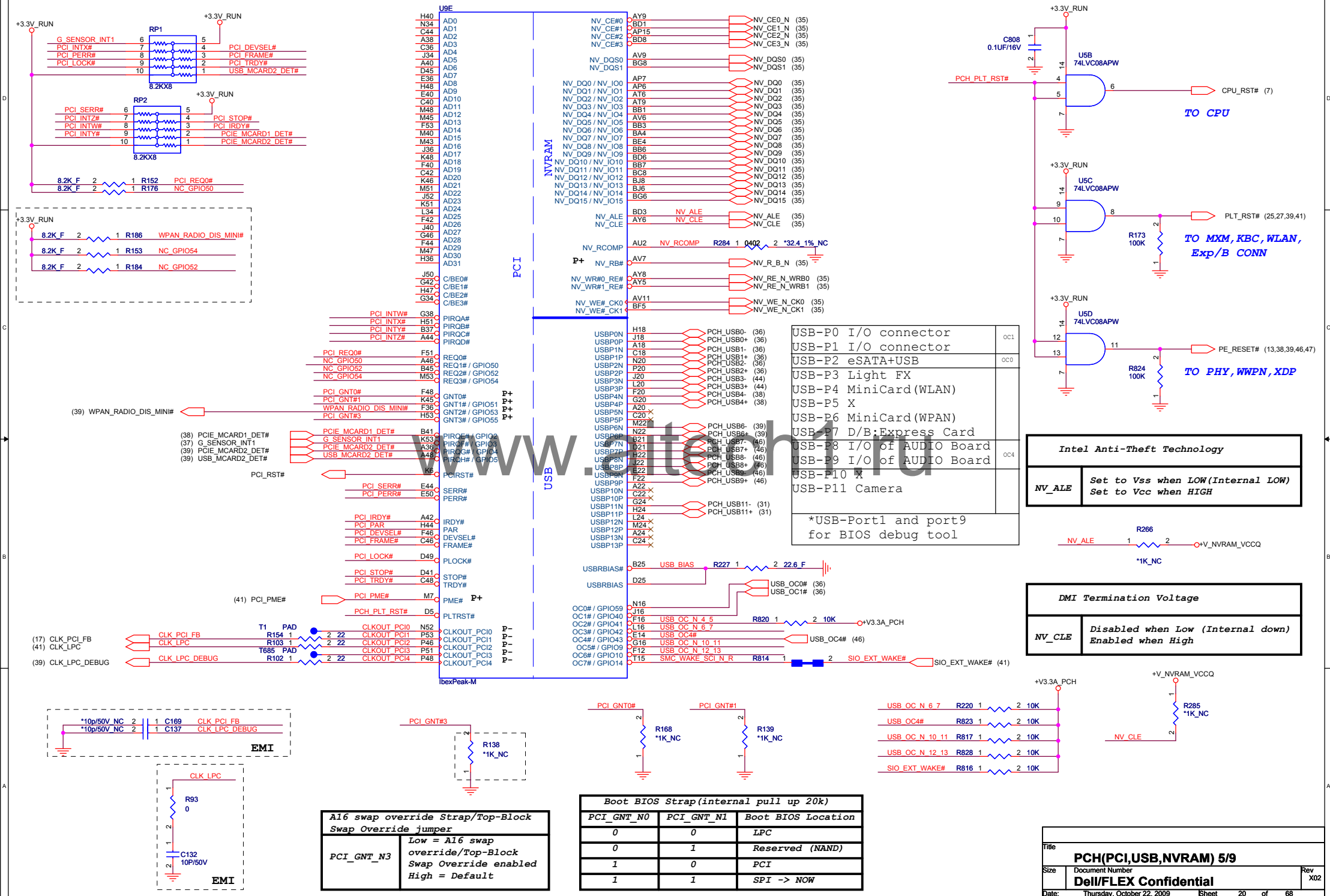


Title			PCH(DMI,FDI,SPM) 3/9		
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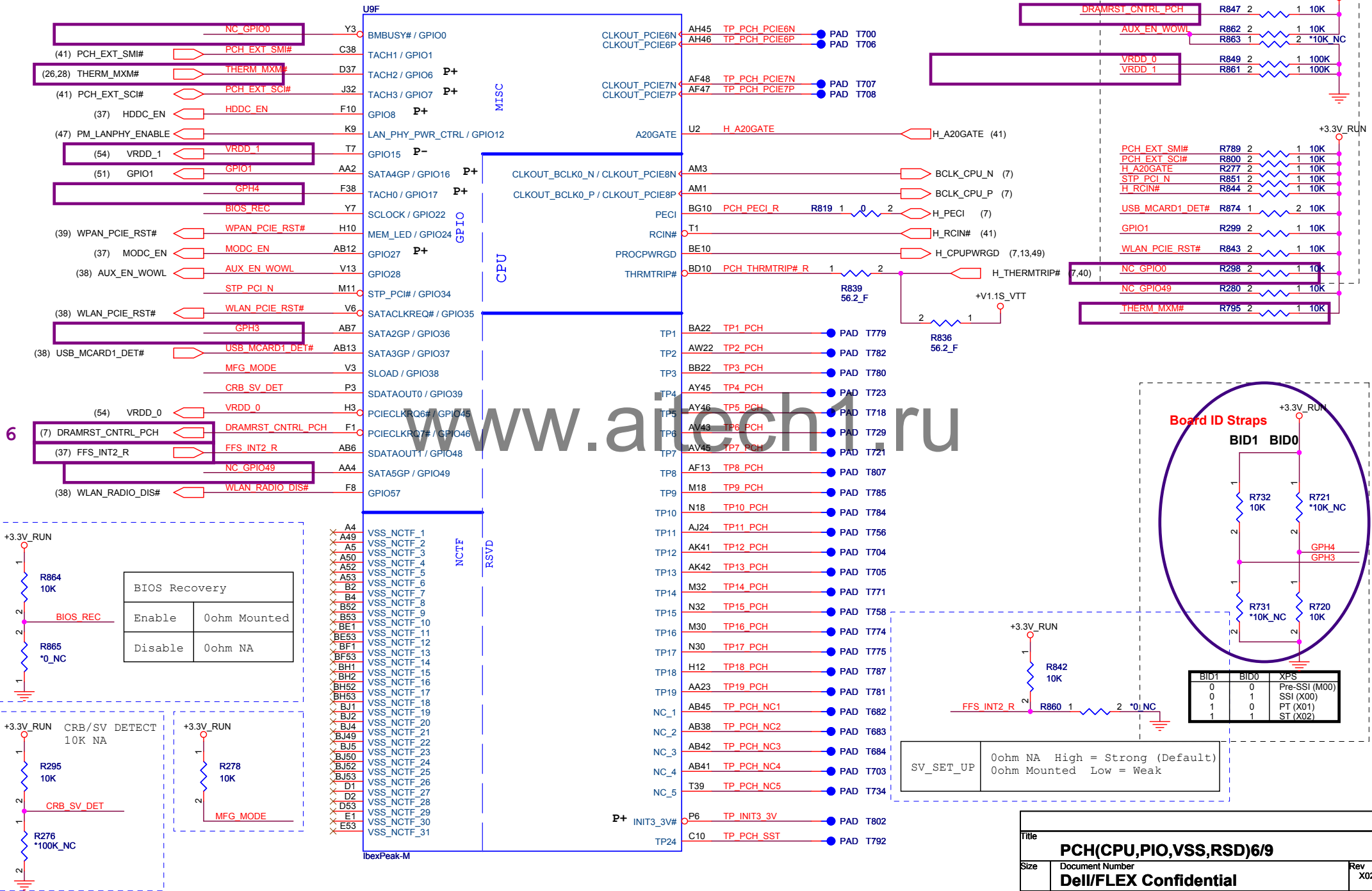
IBEX PEAK-M (LVDS,DDI)



Title		
PCH(CRT,LVDS,DDI) 4/9		
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IBEX PEAK-M (PCI,USB,INTEL(R) TURBO MEMORY)

IBEX PEAK-M(GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M(POWER)

POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

PCI/GPIO/LPC

CPU

RTC

HDA

VCCIO Total
3062mA

VCCSUS3_3 Total
163mA

VCC3_3 Total
357mA

31mA

6mA

VCCME Total
3062mA

Please note that all Ibex Peak-M rails with netnames +V1.1S and +V1.1M rails are actually +V1.05S and +V1.05M rails

1UF*2 pcs for 2 blocks

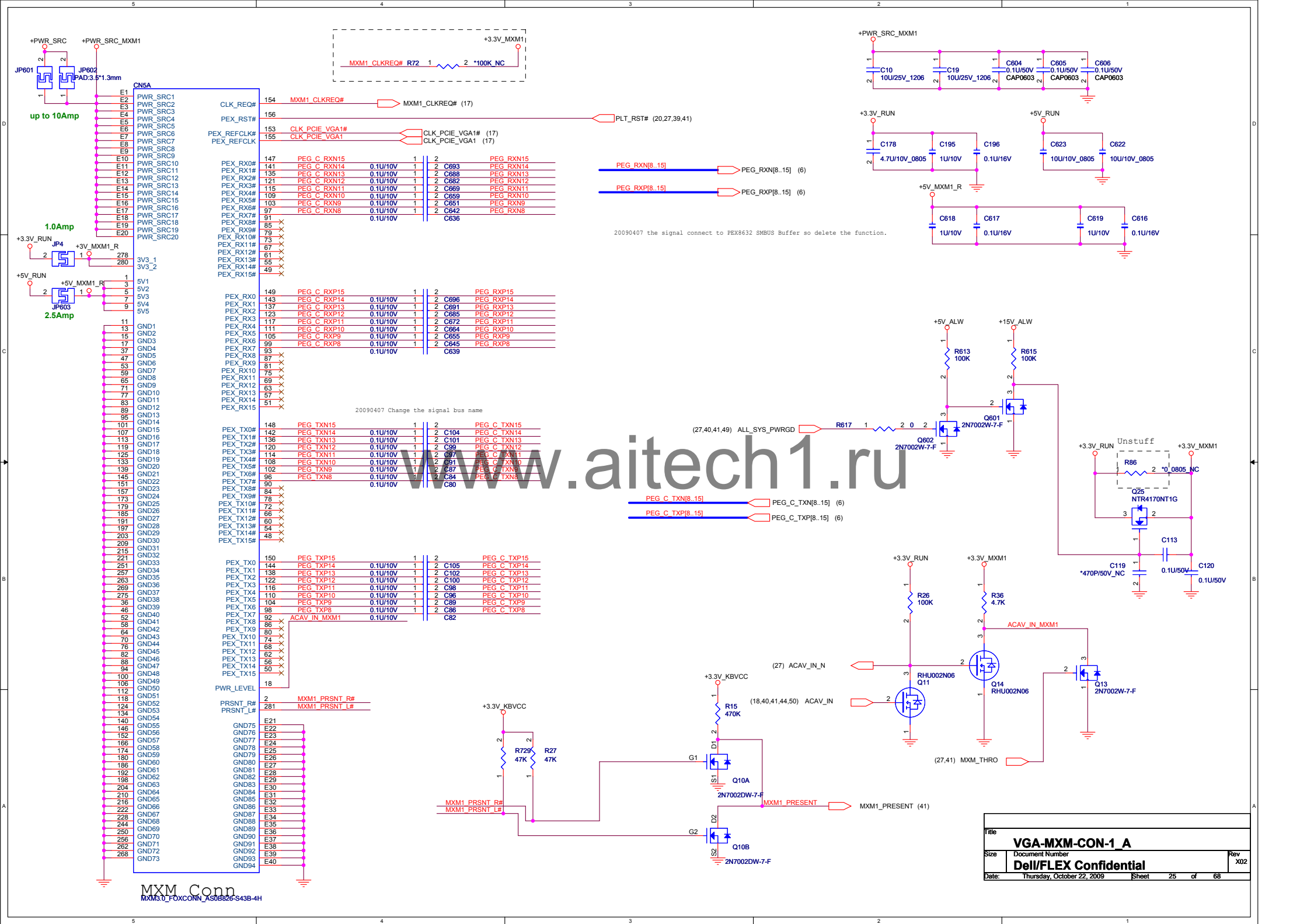
Internal VRM supply

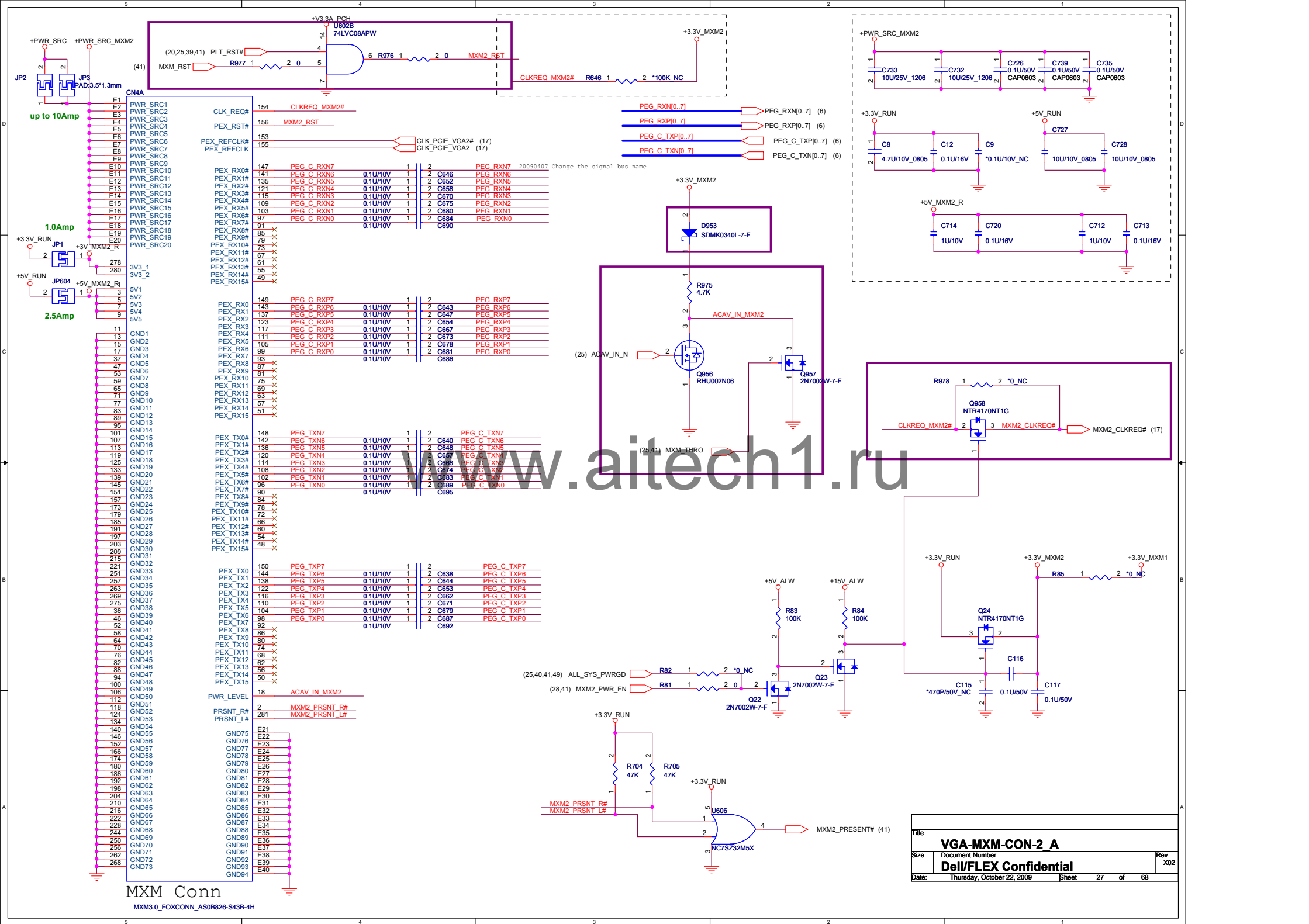
+5V_ALW has off during S4/S5 battery mode.

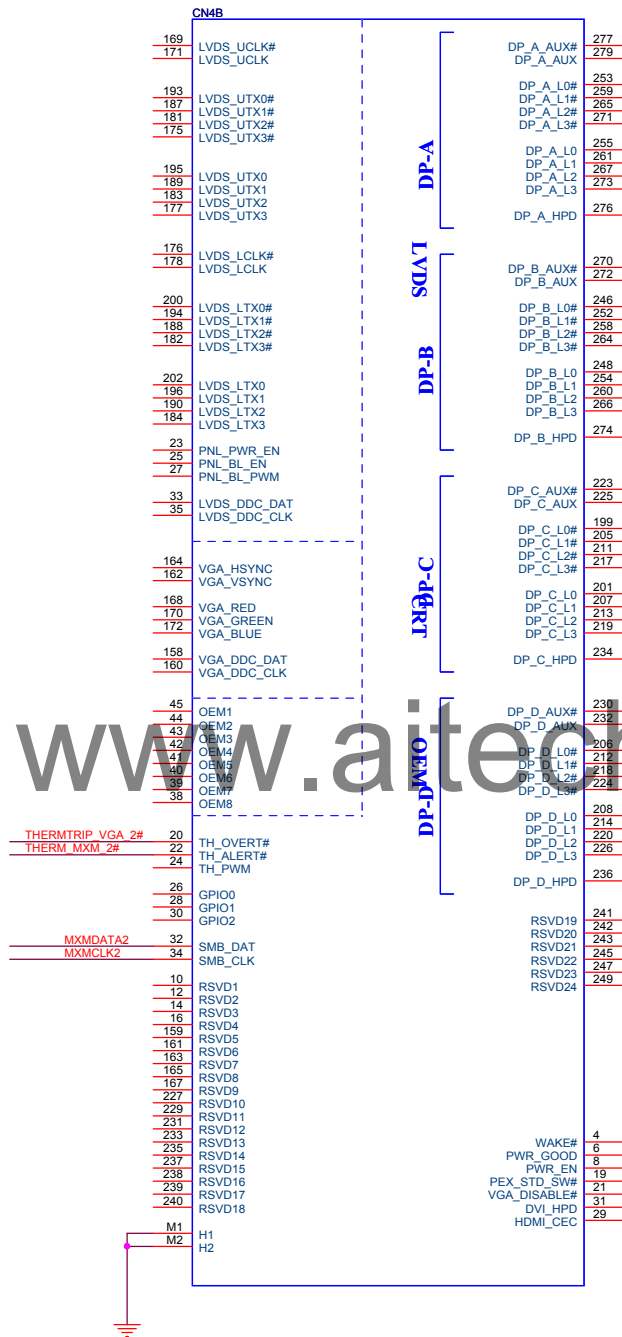
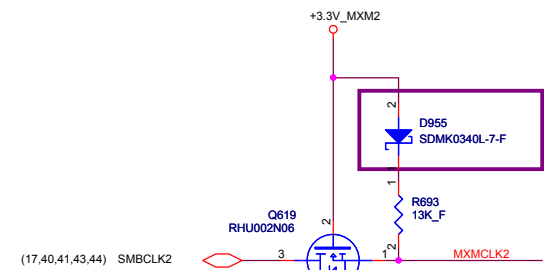
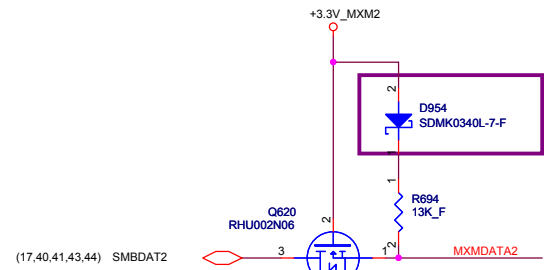
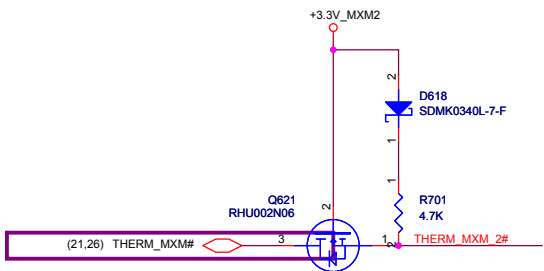
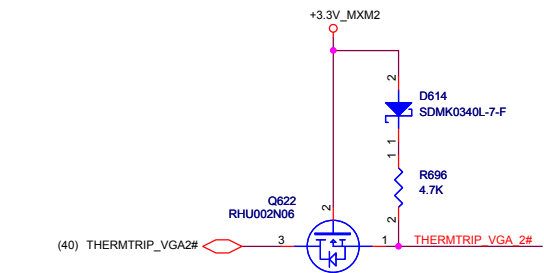
Close to PCH

Internal VRM supply

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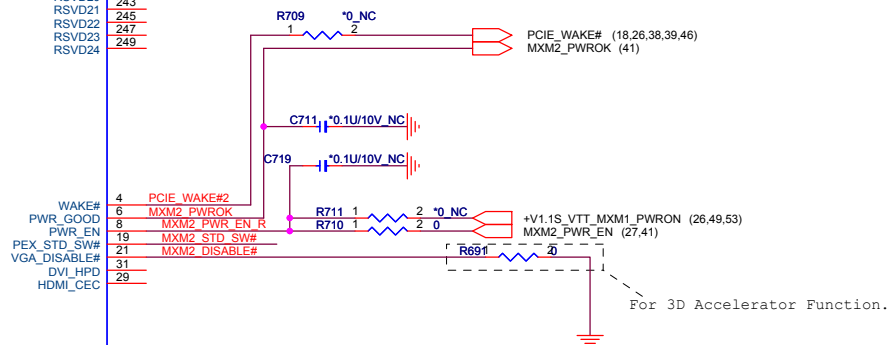
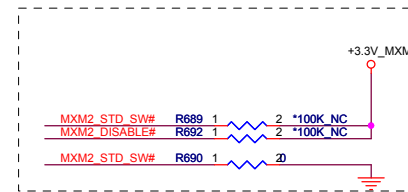






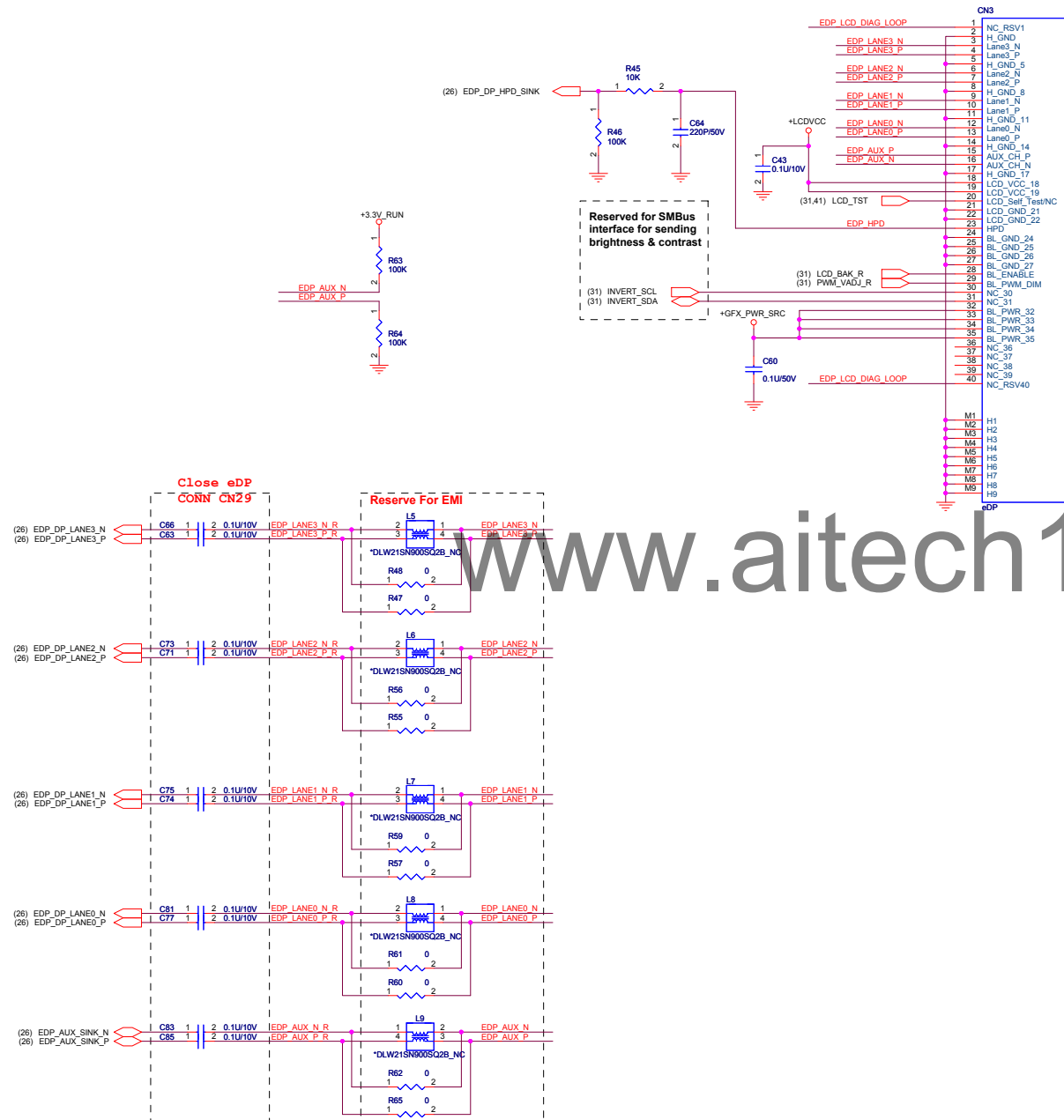
MXM Conn

MXM3.0_FOXCONN_AS0826-S43B-4H



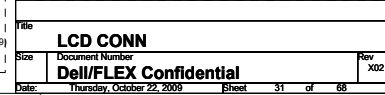
Title		
VGA-MXM-CON-2_B		
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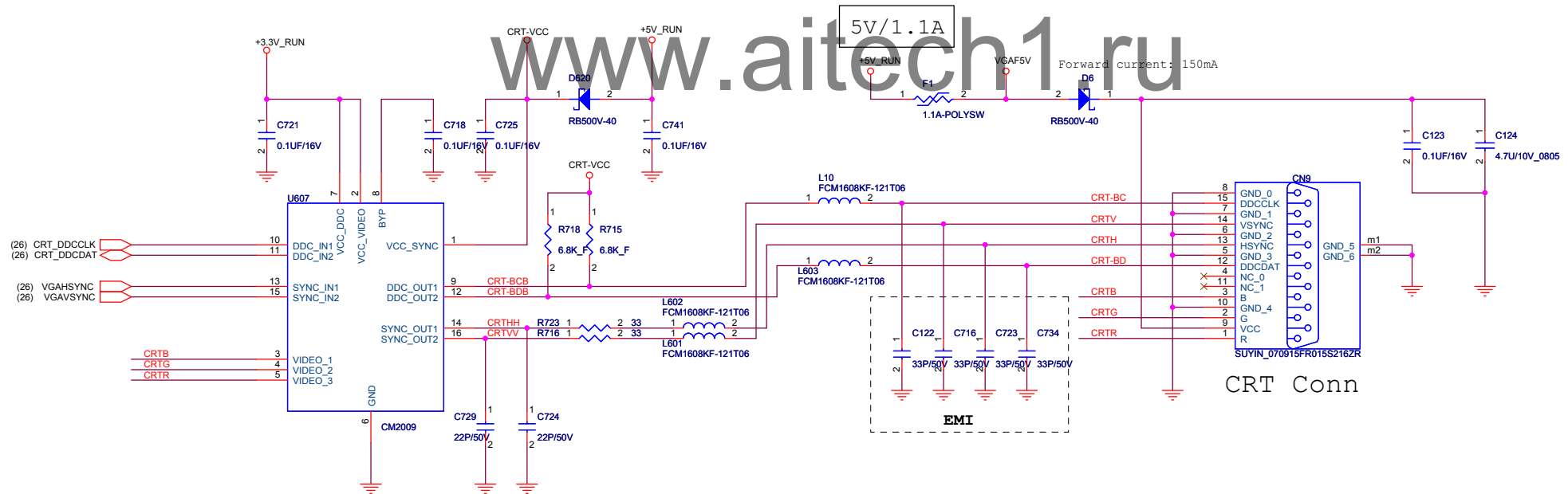
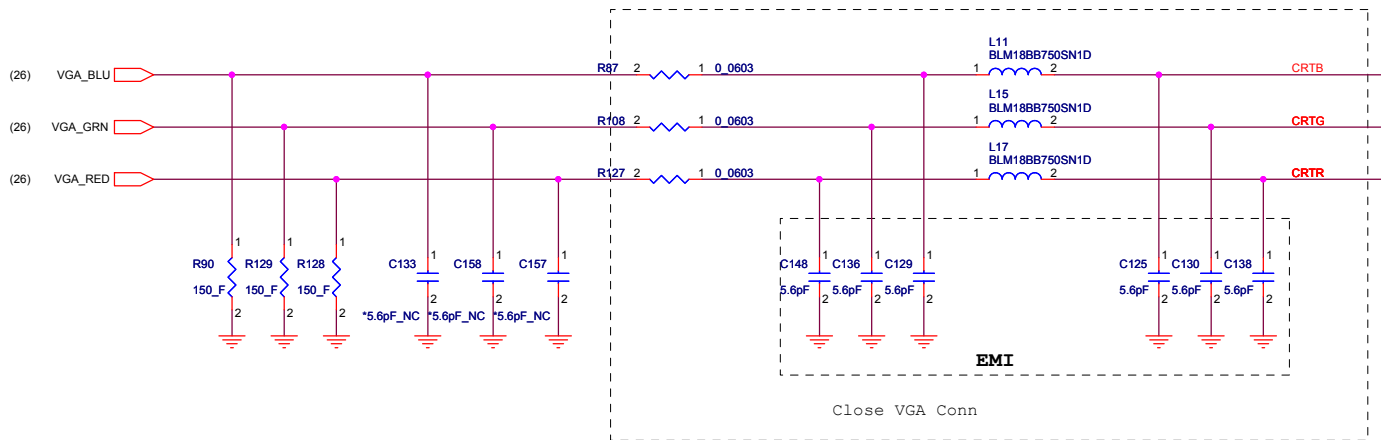
Embedded DISPLAY PORT CONNECTOR



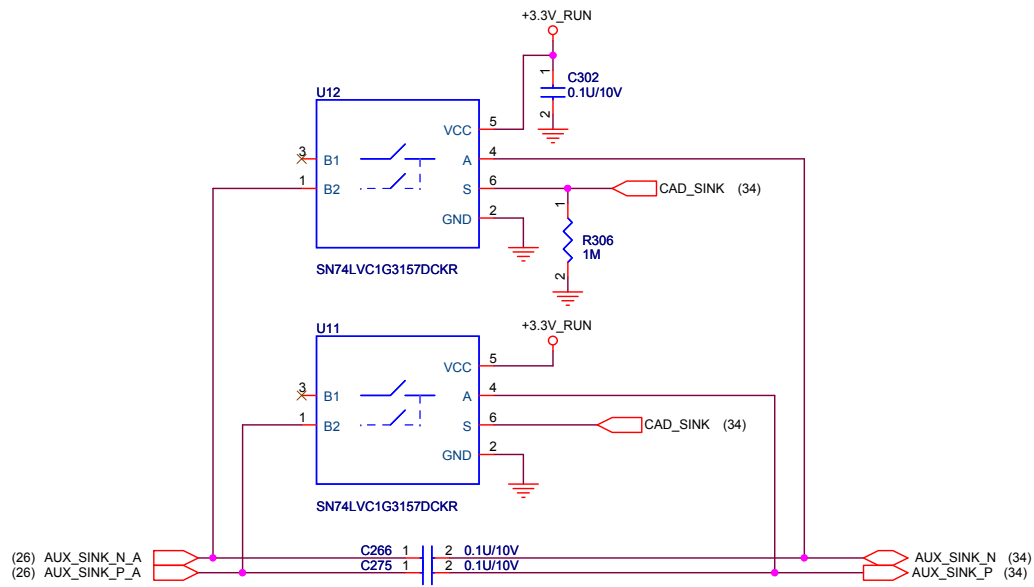
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Title		
HDMI SELECTION		
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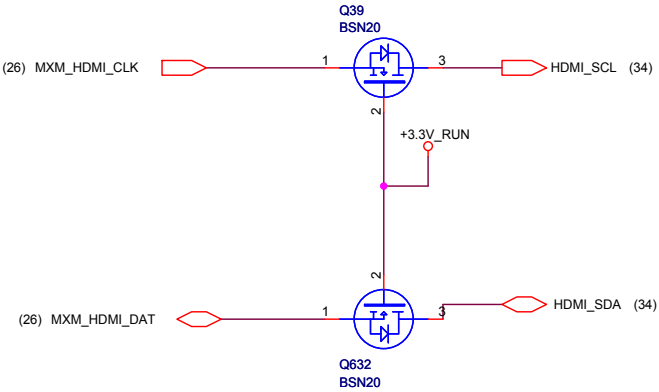




Title			
CRT CONN			
Size	Document Number		Rev
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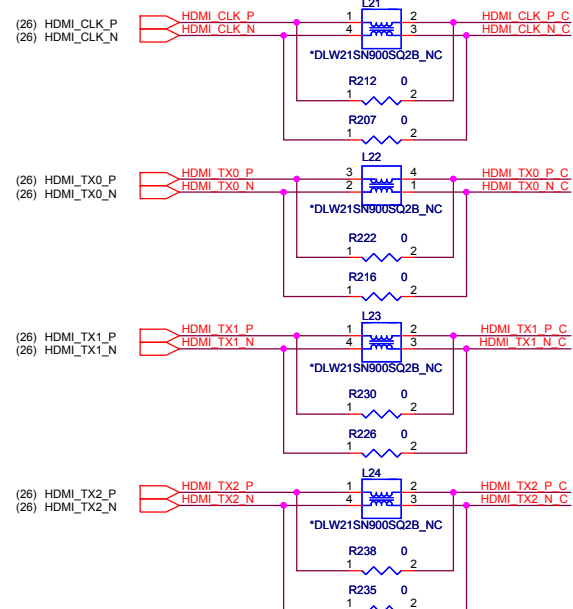


CAD_SINK	SOURCE
L	A=B1 (AC couple)
H	A=B2 (DDC)

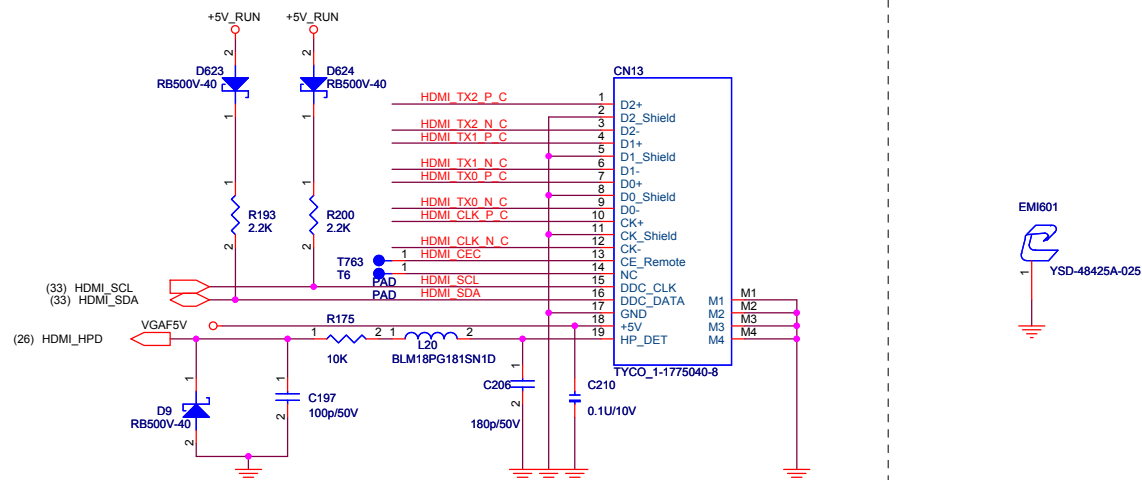


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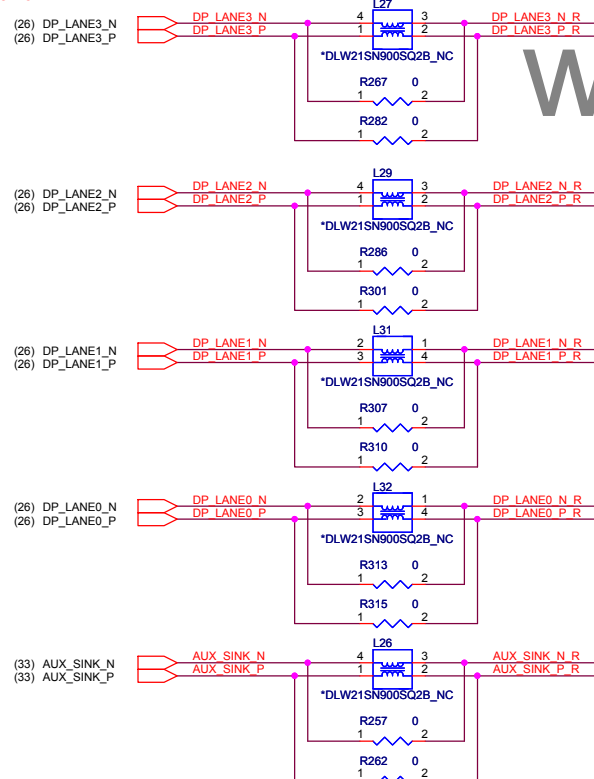
Reserve For EMI



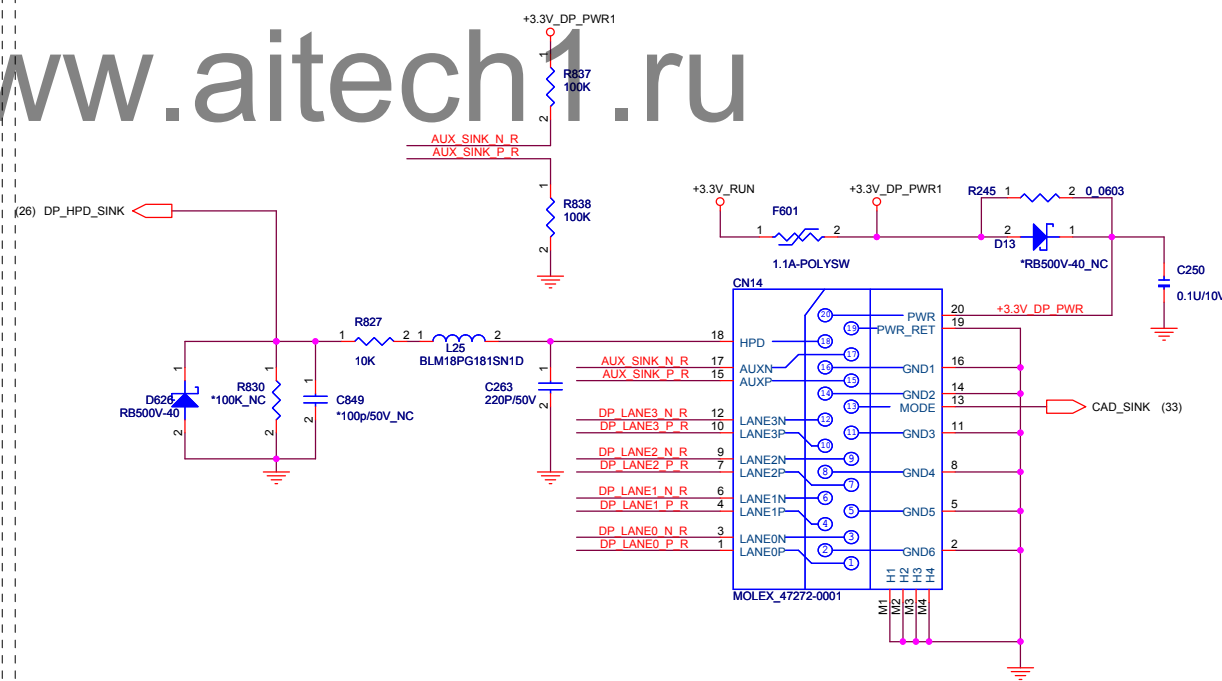
HDMI CONNECTOR



Reserve For EMI

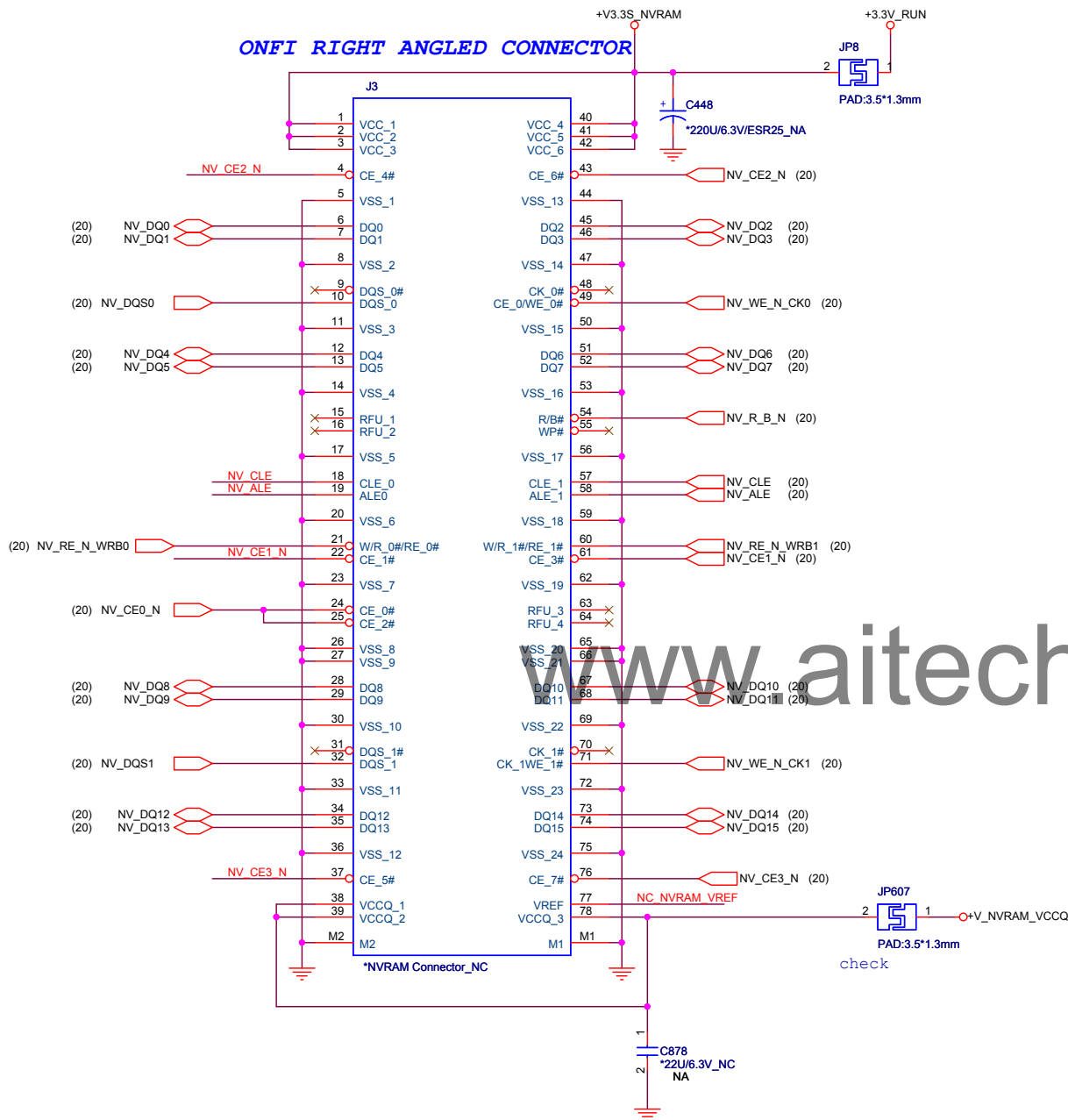


DISPLAY PORT CONNECTOR



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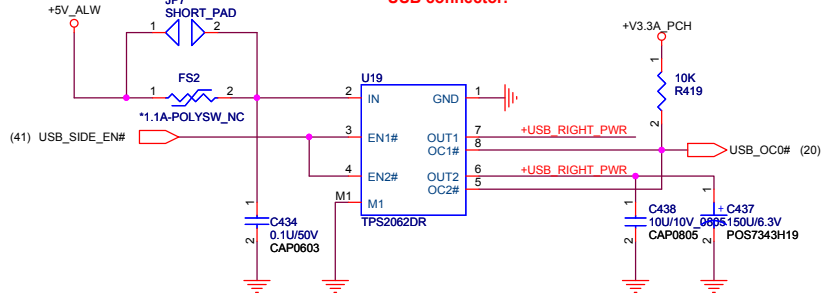
Title			
HDMI & DP CONN			
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Title			
ONFI Connector			
Size	Document Number		Rev
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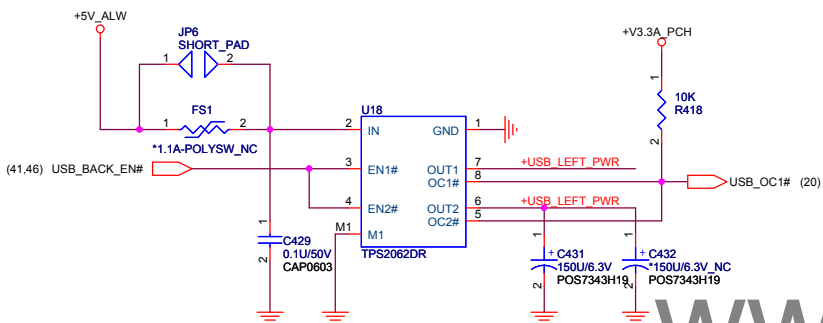
USB POWER SW

Place one 150uF cap by each USB connector. Each channel is 1A



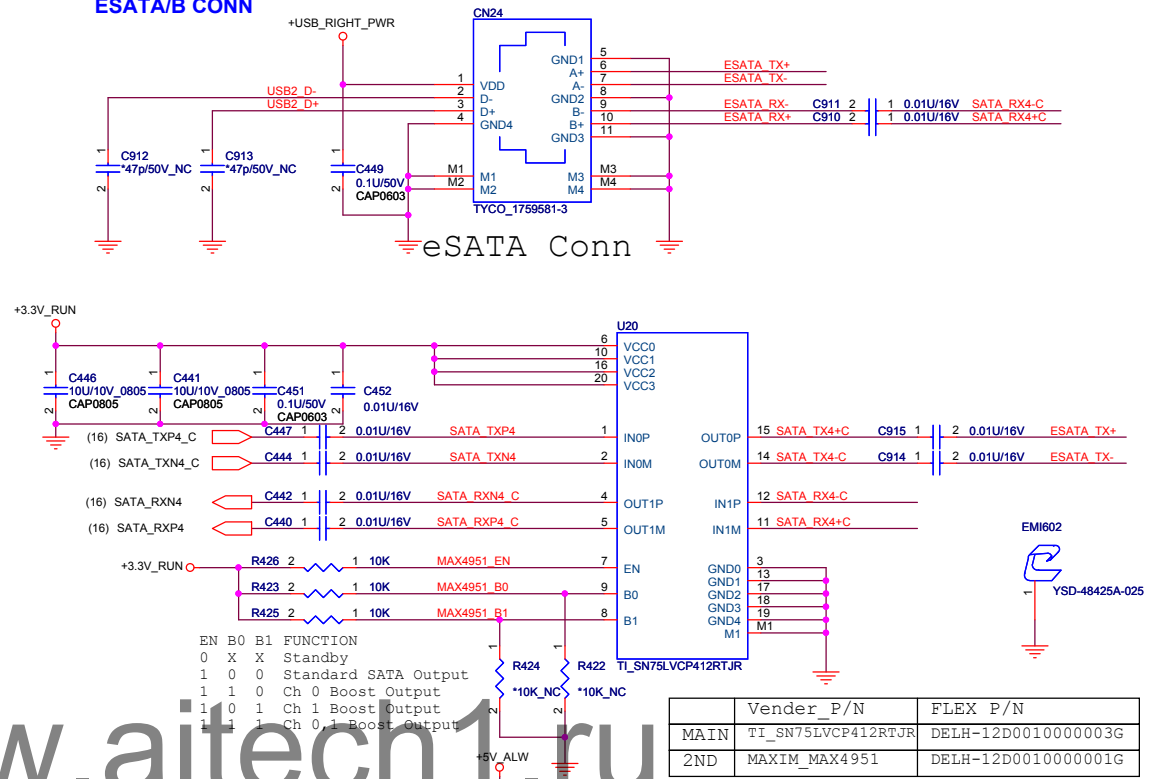
USB POWER SW

Place one 150uF cap by each USB connector. Each channel is 1A



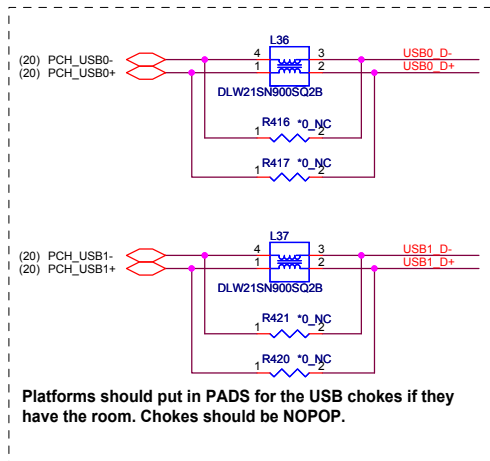
3/24 Neo: Update new symbol

ESATA/B CONN



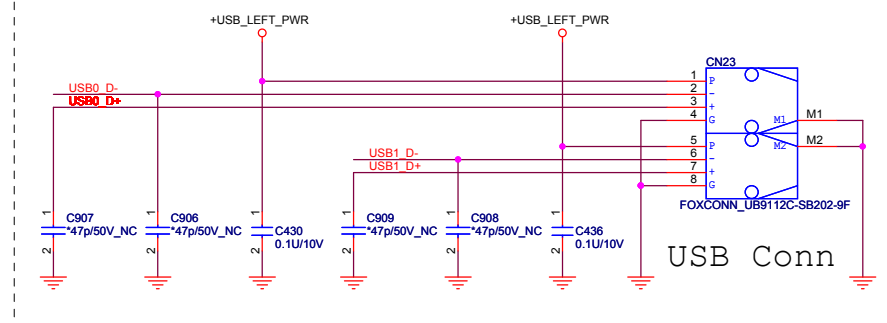
EN B0 B1 FUNCTION
 0 X X Standby
 1 0 0 Standard SATA Output
 1 1 0 Ch 0 Boost Output
 1 0 1 Ch 1 Boost Output
 1 1 1 Ch 0,1 Boost Output

USB_OC0# C435 1 2 47p/50V
 USB_OC1# C433 1 2 47p/50V



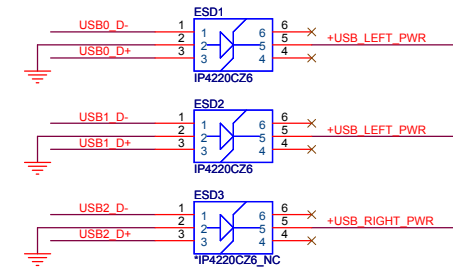
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

USB CONN



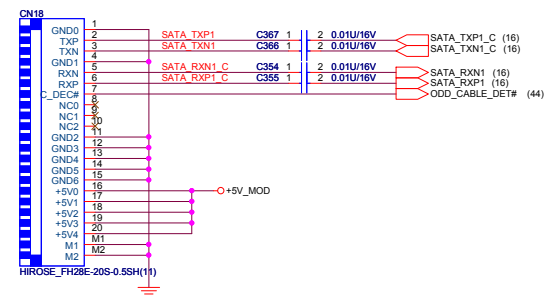
USB Conn

Place ESD diodes as close as USB connector.

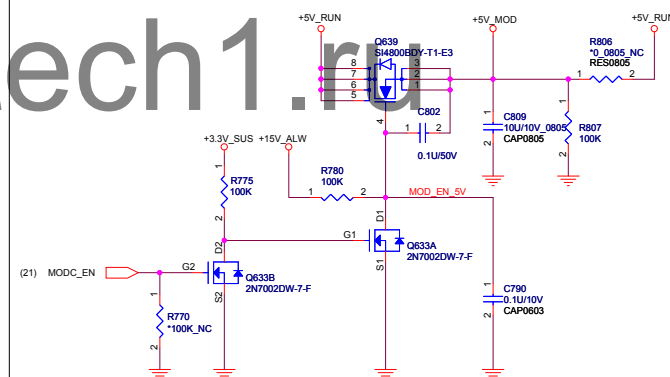
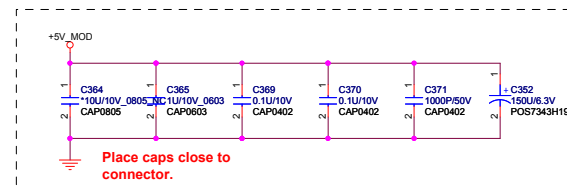


Title		
USBx2 & eSATA		
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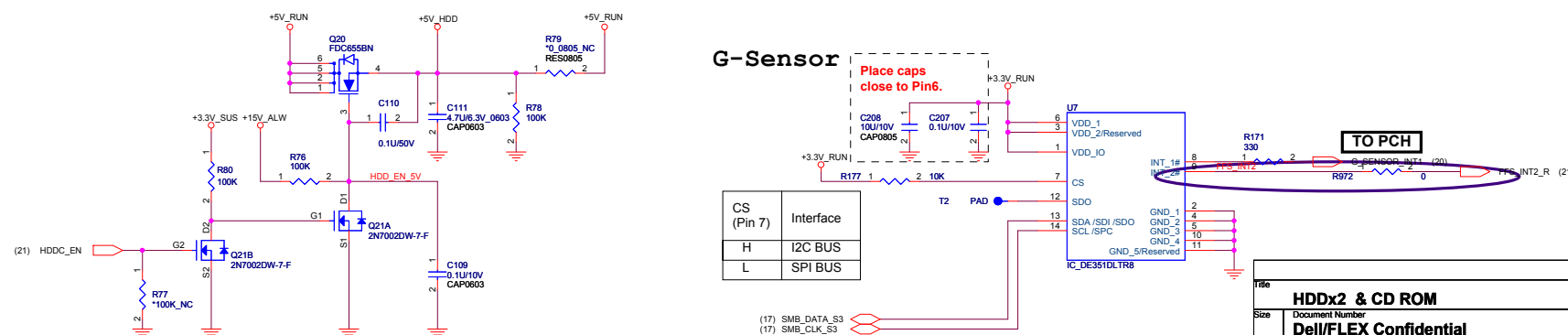
Slave HDD Conn



ODD Conn



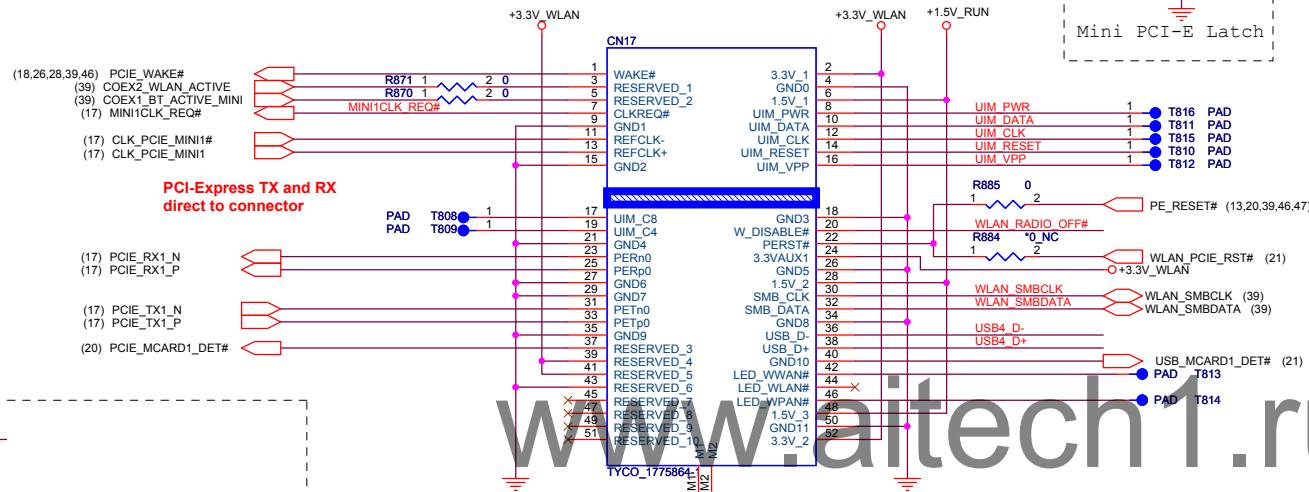
G-Sensor



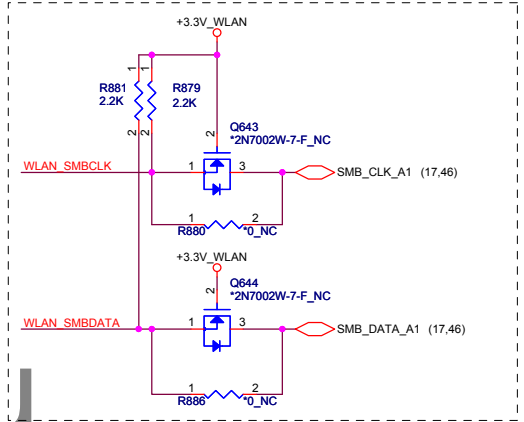
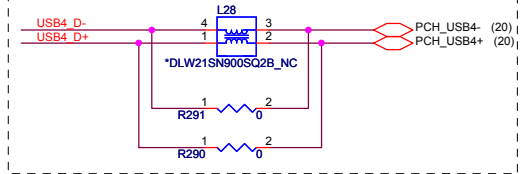
CS (Pin 7)	Interface
H	I2C BUS
L	SPI BUS

Title HDDx2 & CD ROM			
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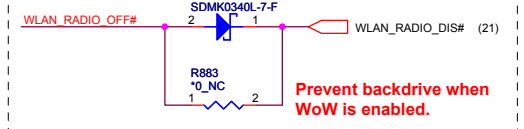
MiniCard WMAX Connector



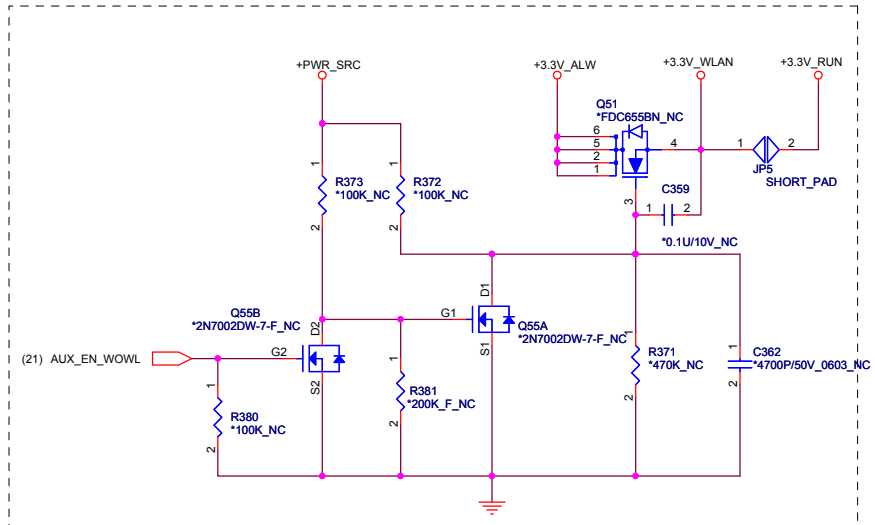
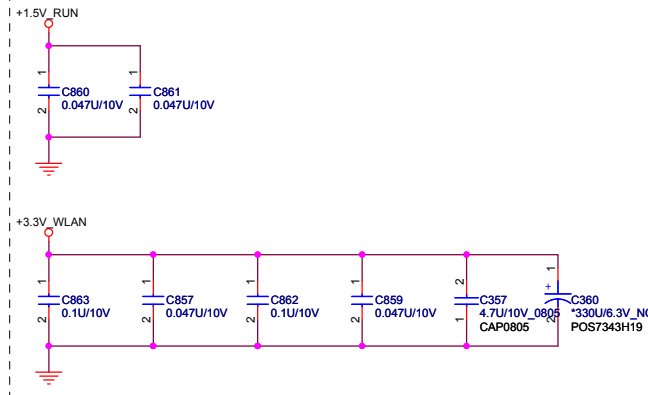
Reserved PAD for EMI



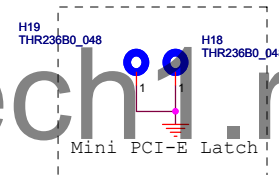
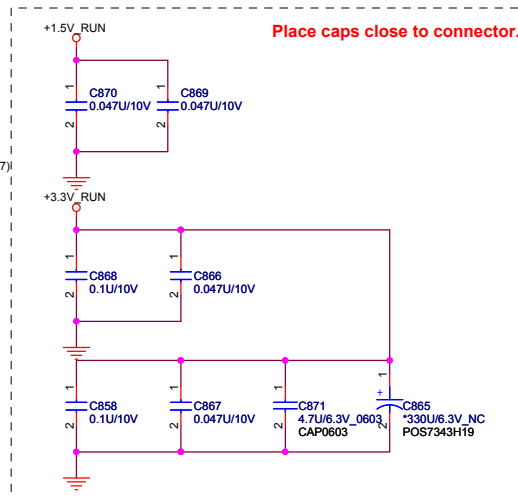
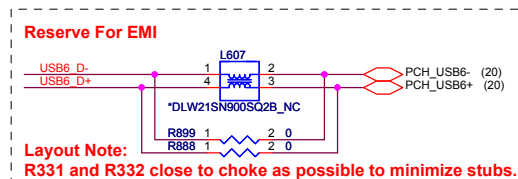
Support for WoW

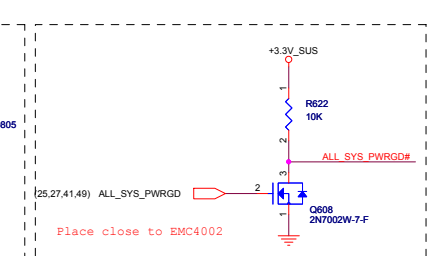
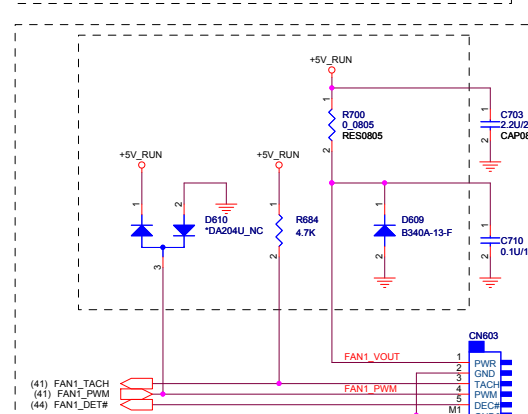
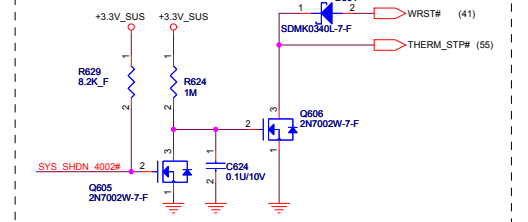
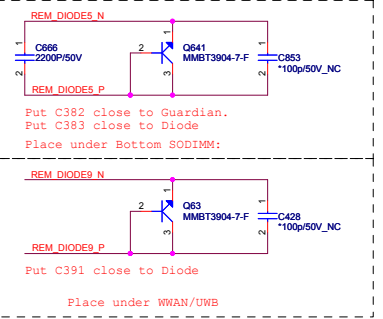
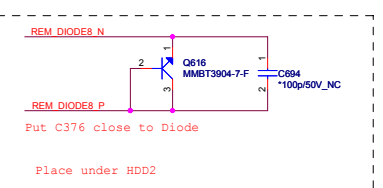


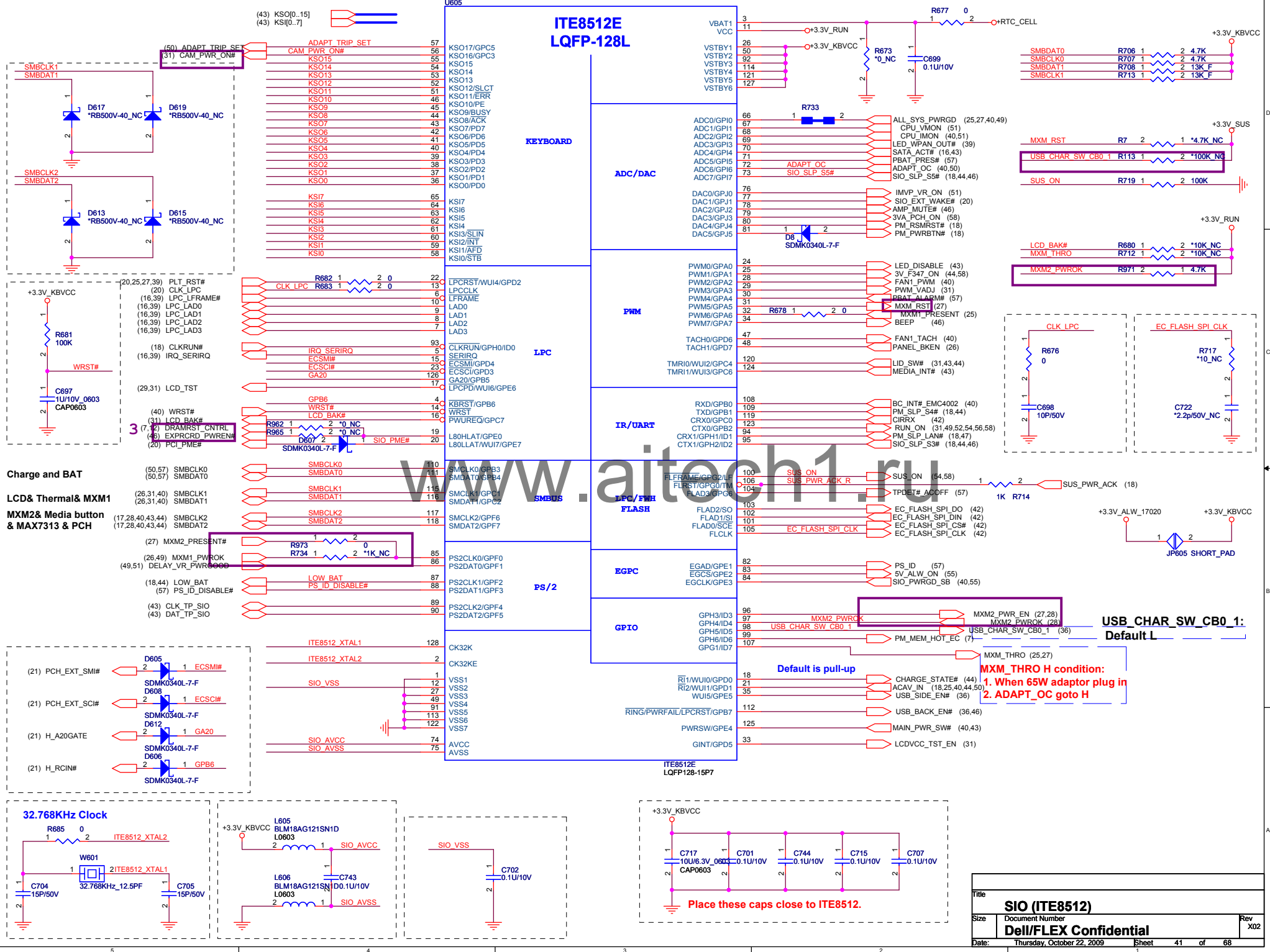
Place caps close to connector.

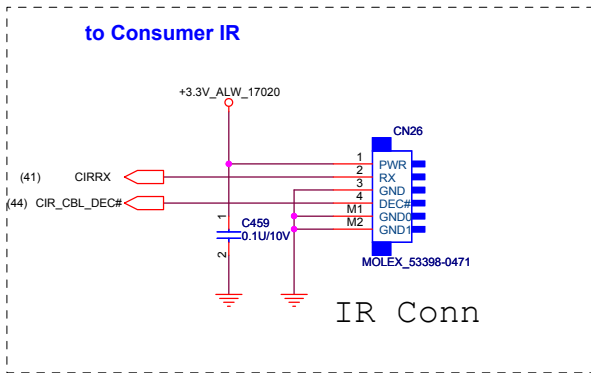
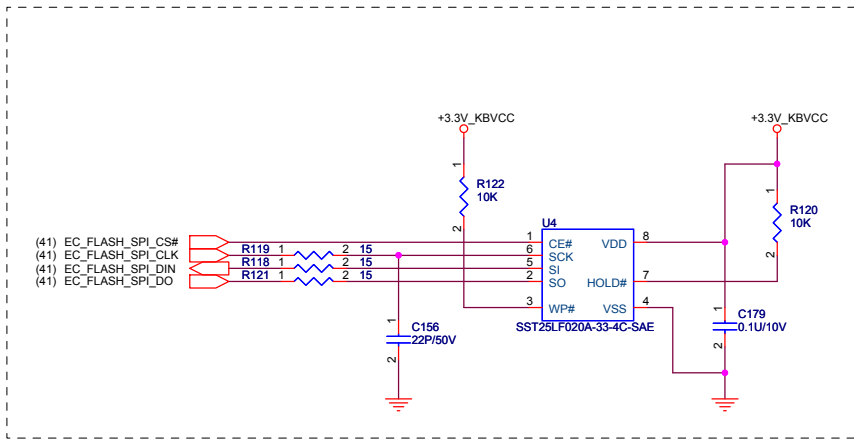


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MINI-CARD(WiMax)		
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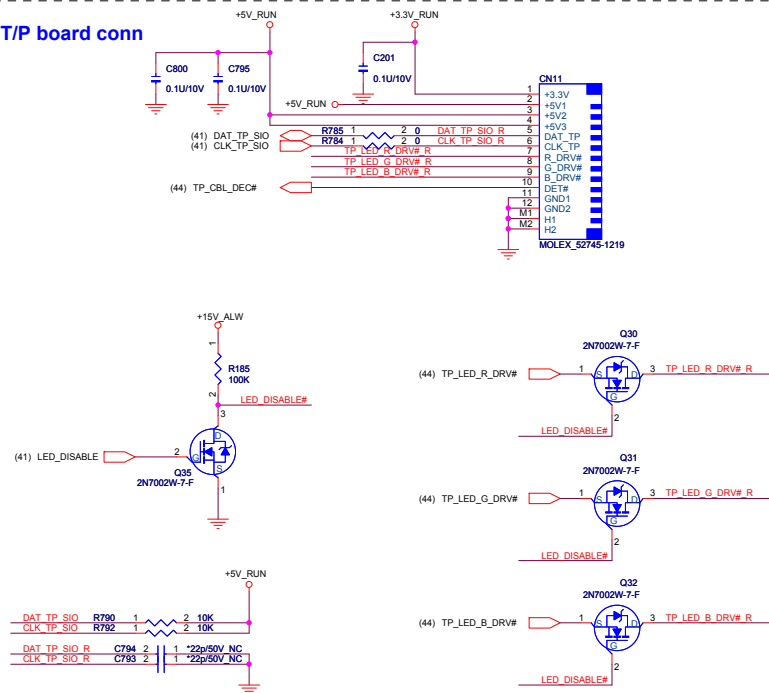




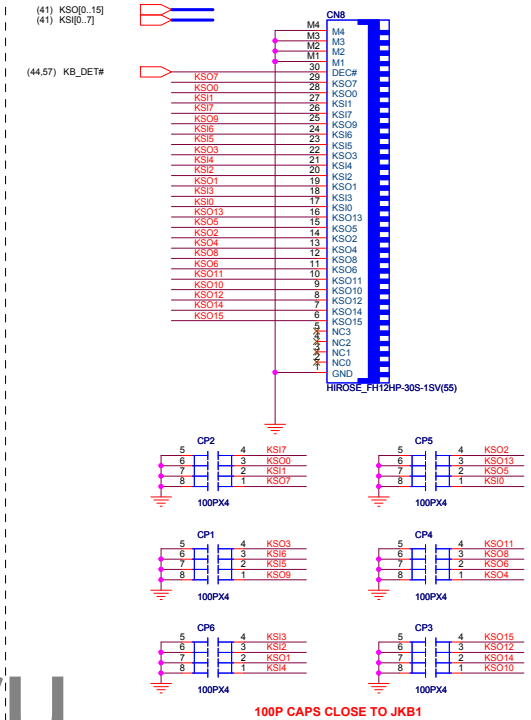


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T/P board conn

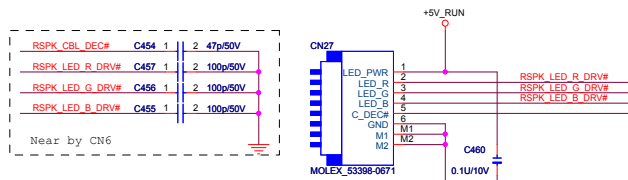


KEYBOARD CONNECTOR

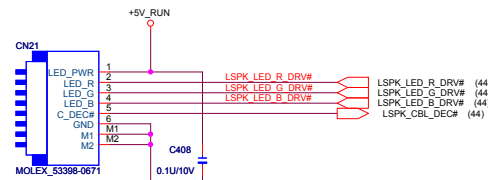


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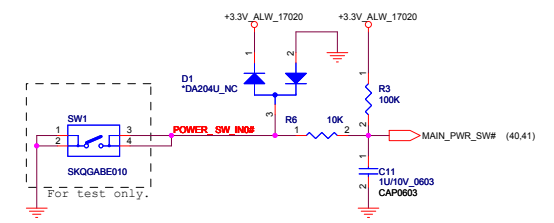
Right SPK LED Conn



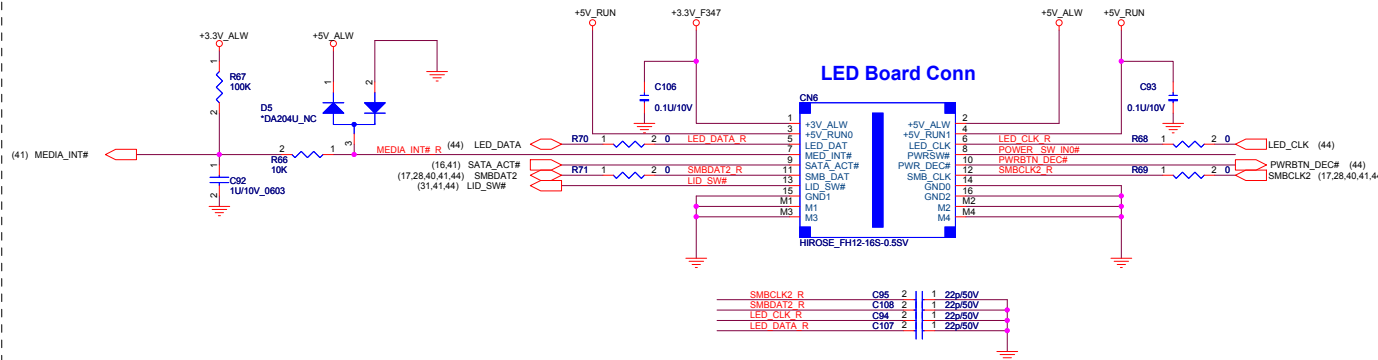
Left SPK LED Conn

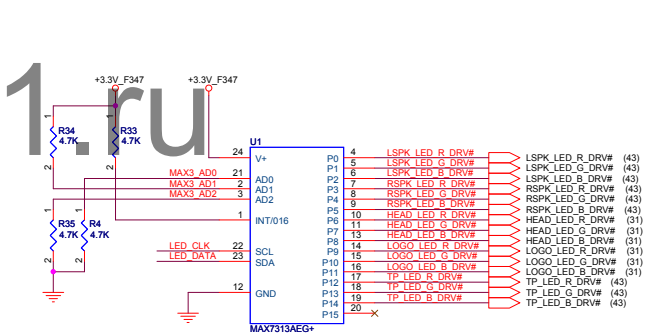
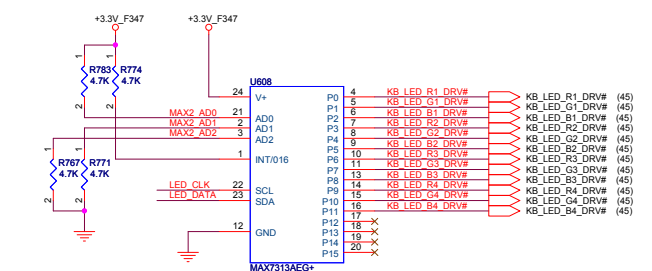
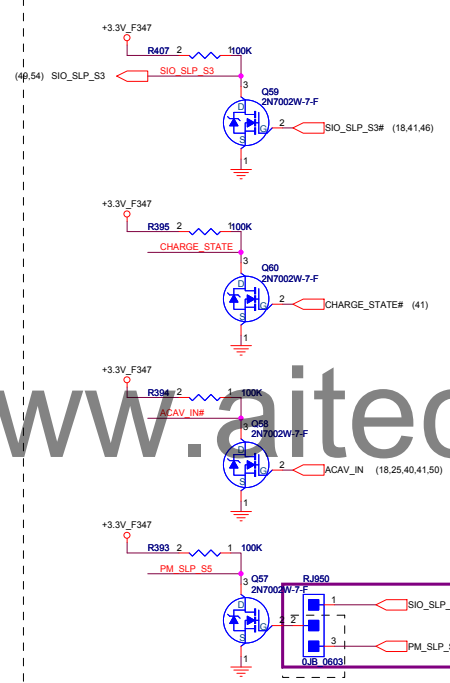
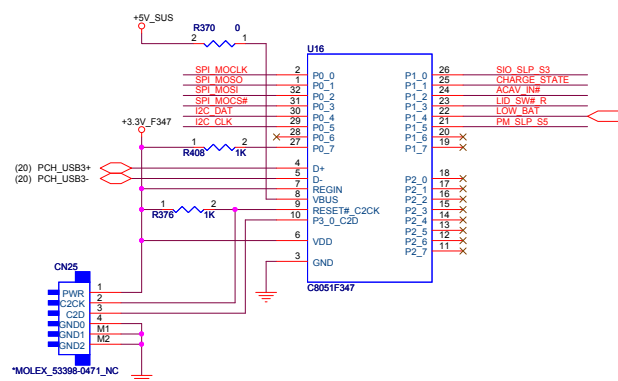
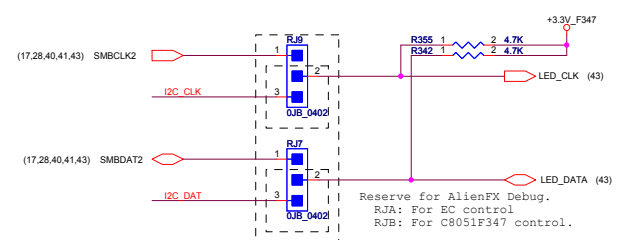
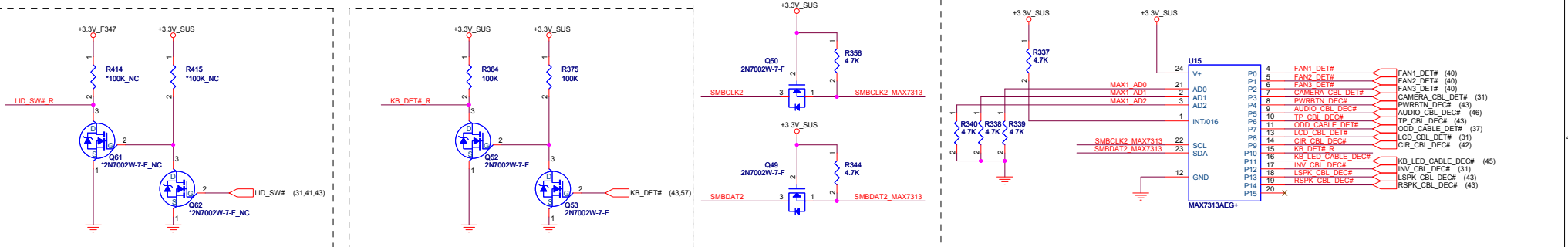


Power Button



LED Board Conn

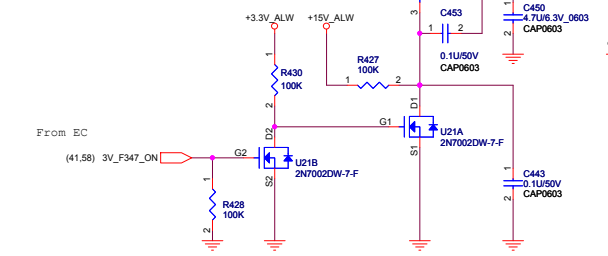
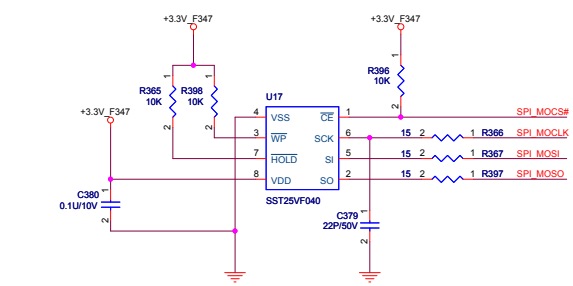




3.3V_F347 behavior

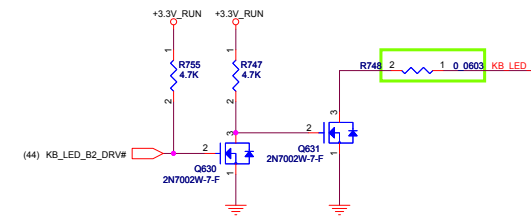
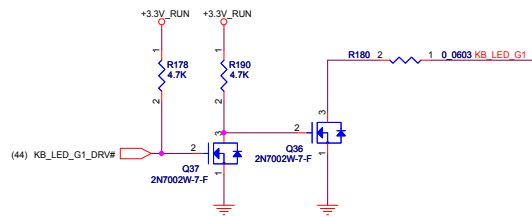
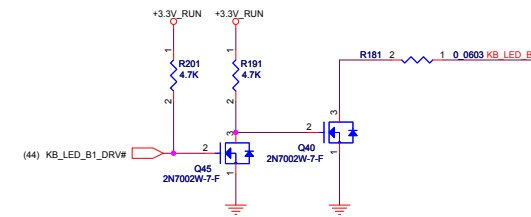
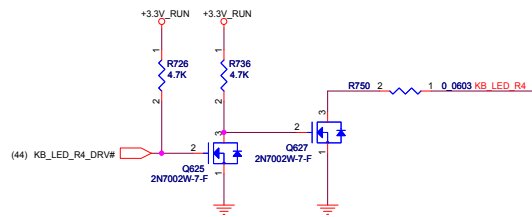
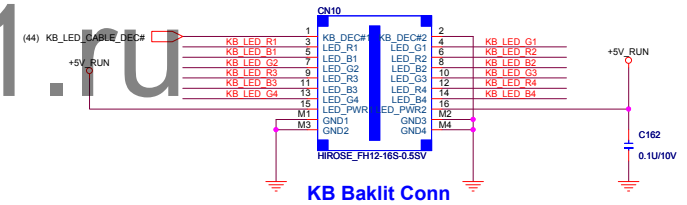
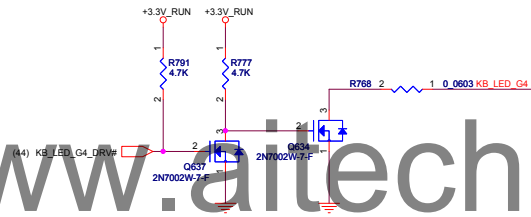
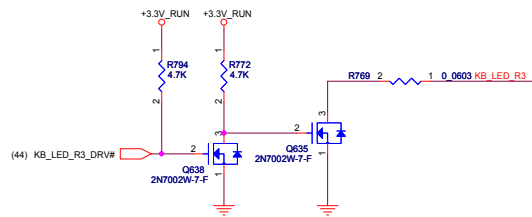
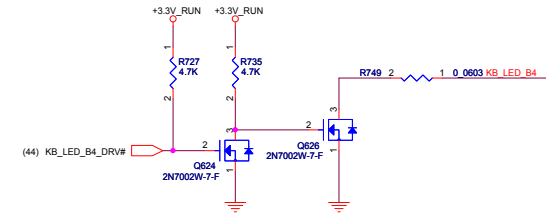
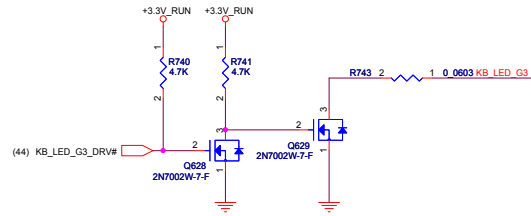
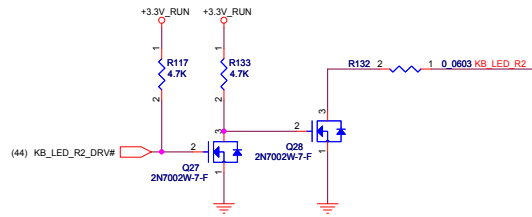
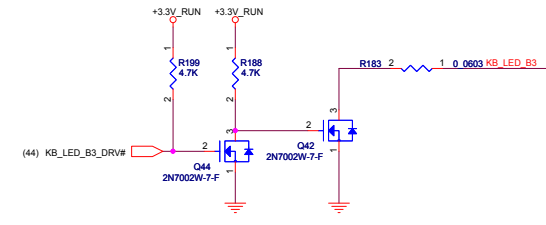
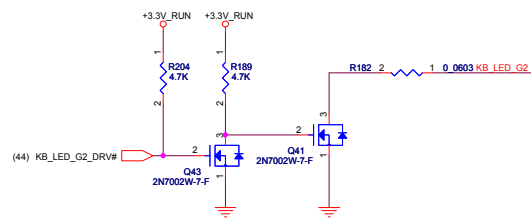
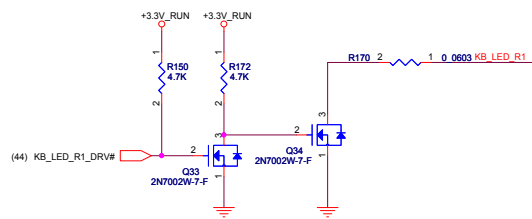
	S0	S3	S4	S5
AC In	ON	ON	ON	ON
BAT only	ON	ON	Off	Off

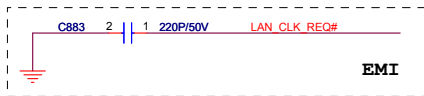
AC mode Battery full in S5:
turn off ELC controller.



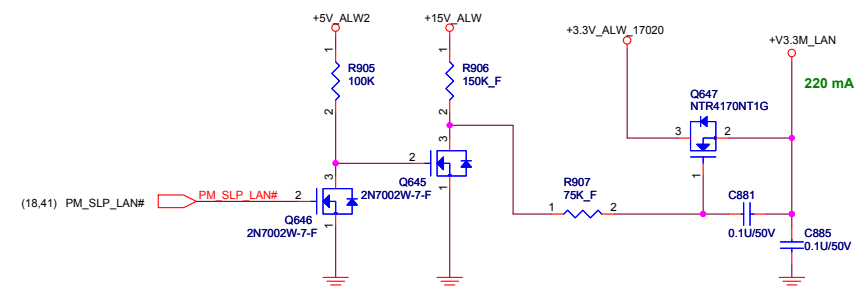
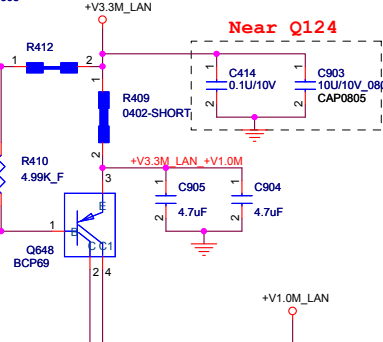
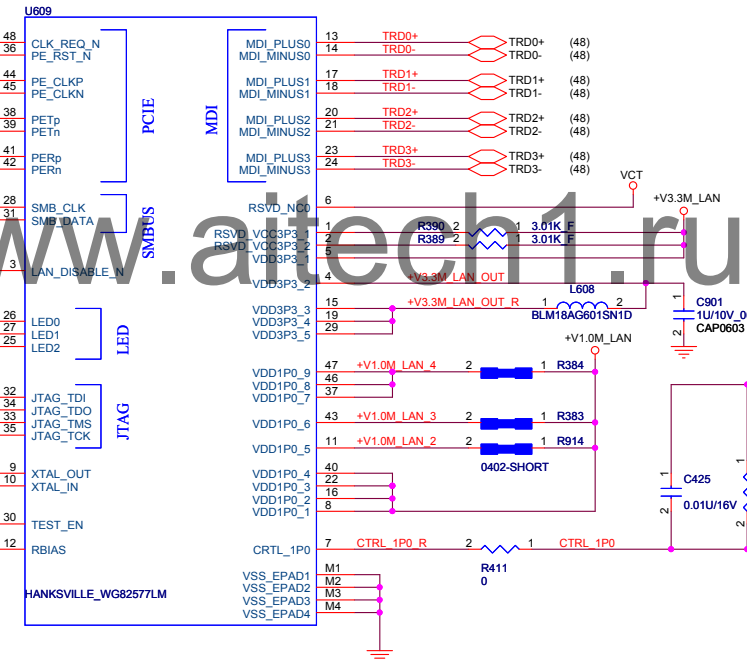
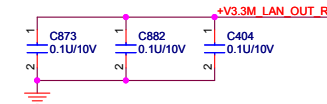
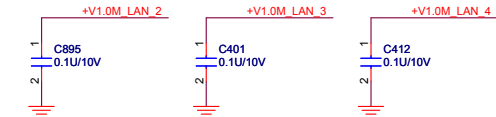
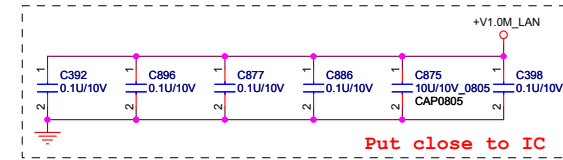
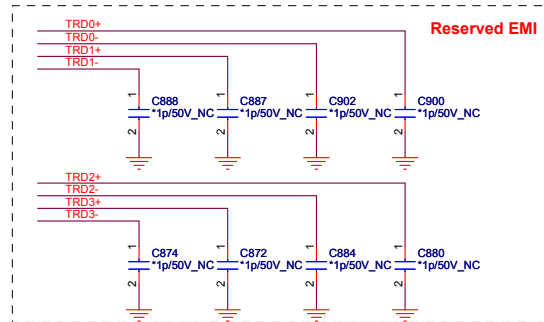
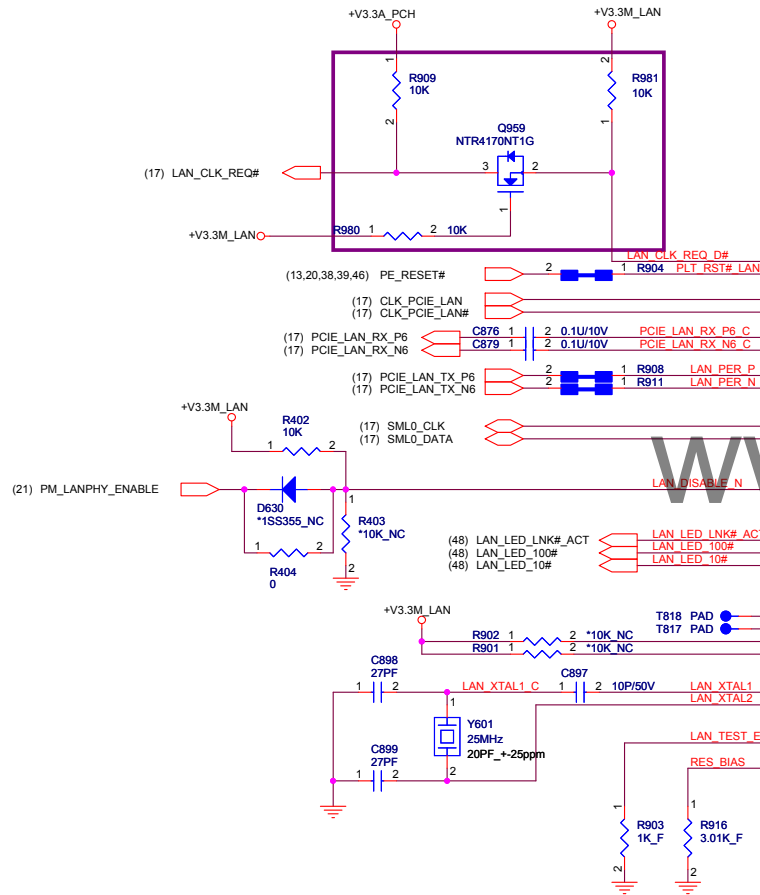
Reference	AD2	AD1	AD0	MAX7313 #
U41	0	0	0	Cable Detect#
U43	0	0	1	KB LED
U45	0	1	0	SPKs Heads Logo& T/P LED
---	0	1	1	LED Board
---	1	0	0	Media Board
---	1	0	1	Media Board

Reference	AD2	AD1	AD0	MAX7313 #
CAMERA_CBL_DET#	R354	1	2	100K
AUDIO_CBL_DET#	R362	1	2	100K
TP_CBL_DET#	R368	1	2	100K
ODD_CABLE_DET#	R374	1	2	100K
LCD_CBL_DET#	R383	1	2	100K
CIR_CBL_DET#	R391	1	2	100K
KB_LED_CABLE_DET#	R397	1	2	100K
FAN1_DET#	R343	1	2	100K
FAN2_DET#	R347	1	2	100K
FAN3_DET#	R352	1	2	100K
INV_CBL_DET#	R353	1	2	100K
LSPK_CBL_DET#	R346	1	2	100K
RSPK_CBL_DET#	R346	1	2	100K
PWRBTN_DEC#	R358	1	2	100K





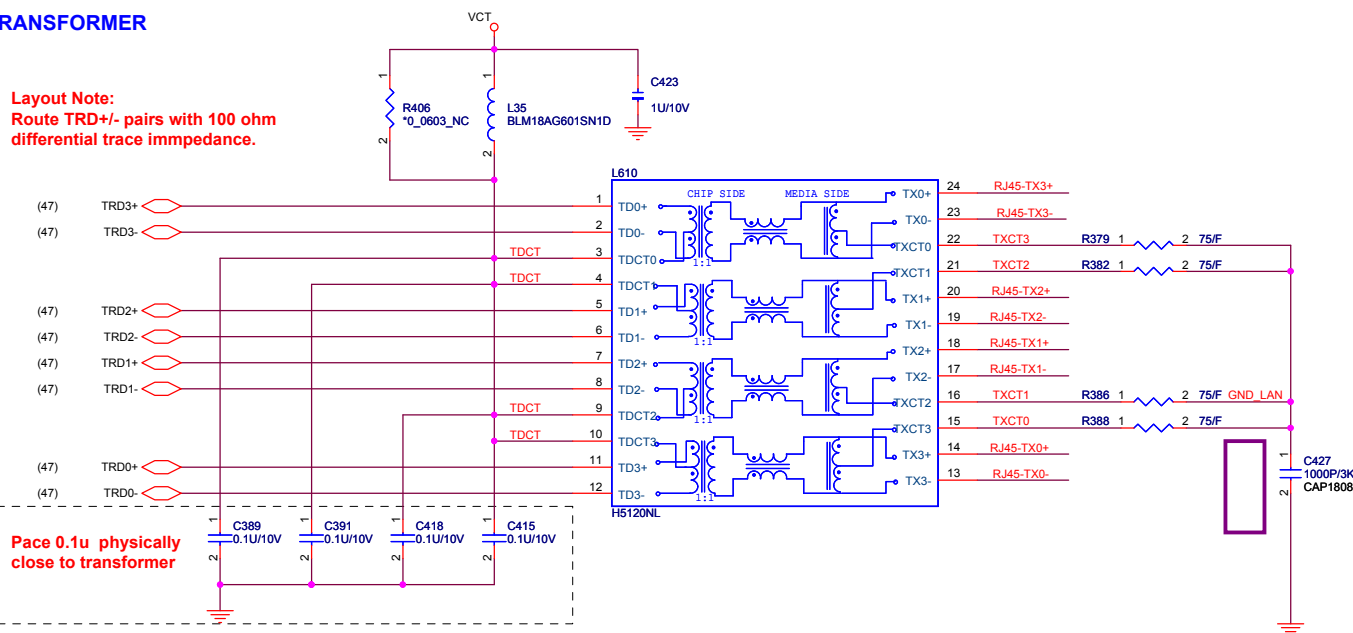
Hanksville PHY	FLEX P/N
WG82577LC QKPN	DELH-10D0040000005G



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PHY HANKSVILLE GbE LAN		
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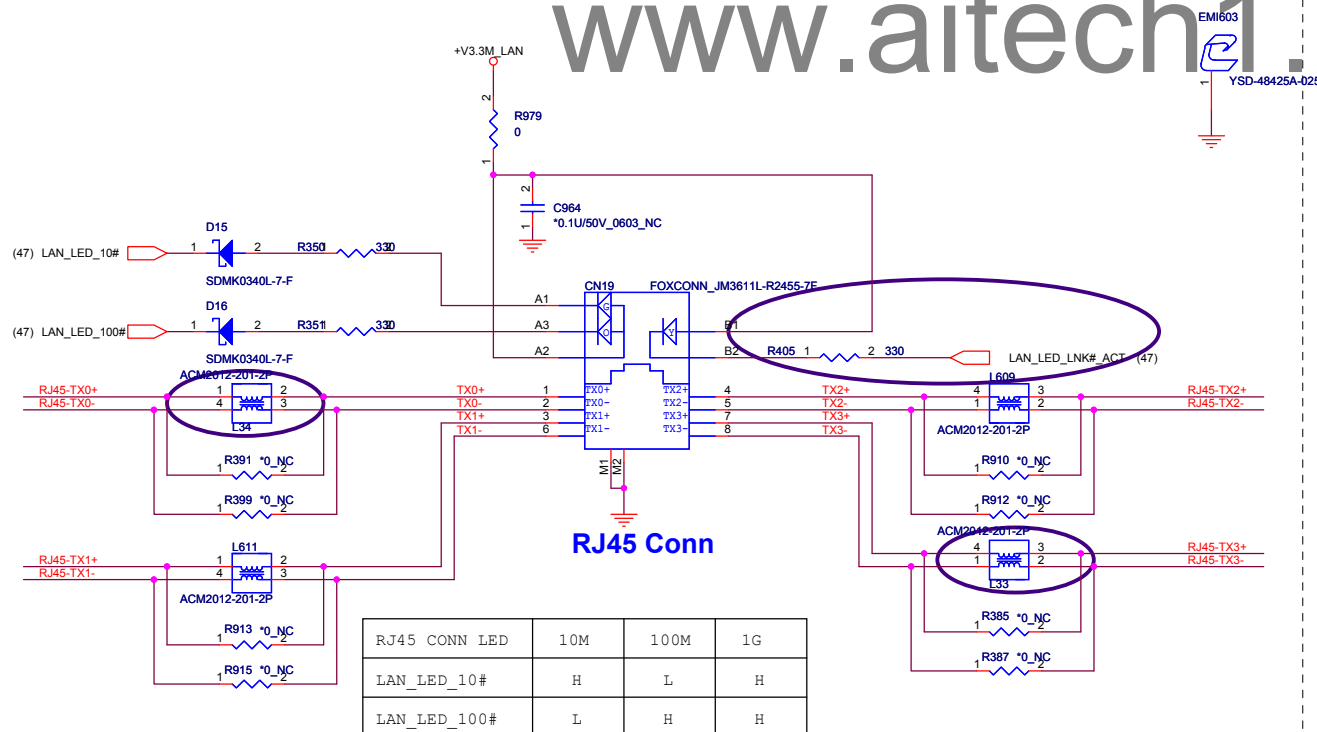
TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



Place 0.1u physically close to transformer

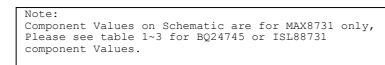
RJ-45 Connector

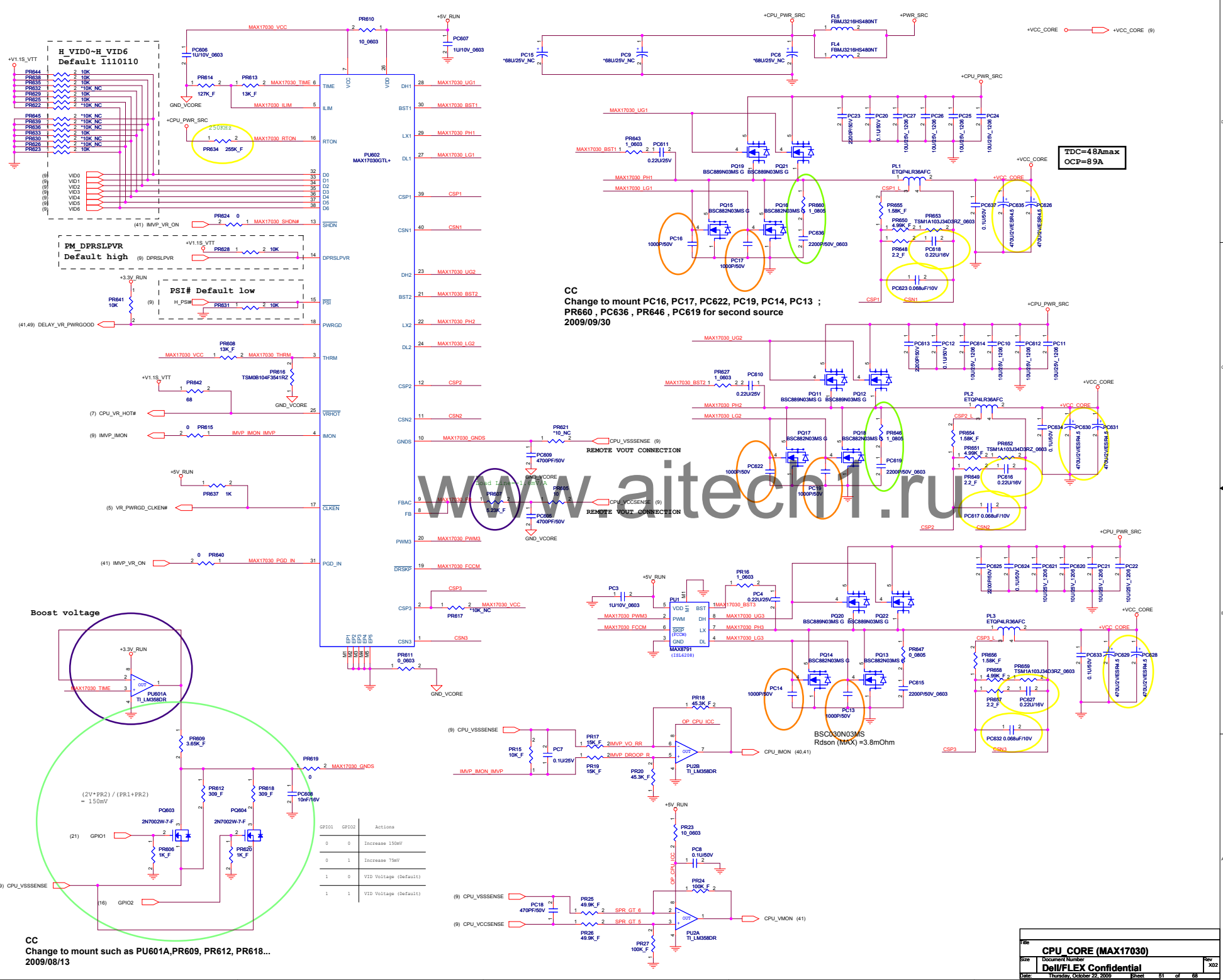


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RJ45 CONN LED	10M	100M	1G
LAN_LED_10#	H	L	H
LAN_LED_100#	L	H	H

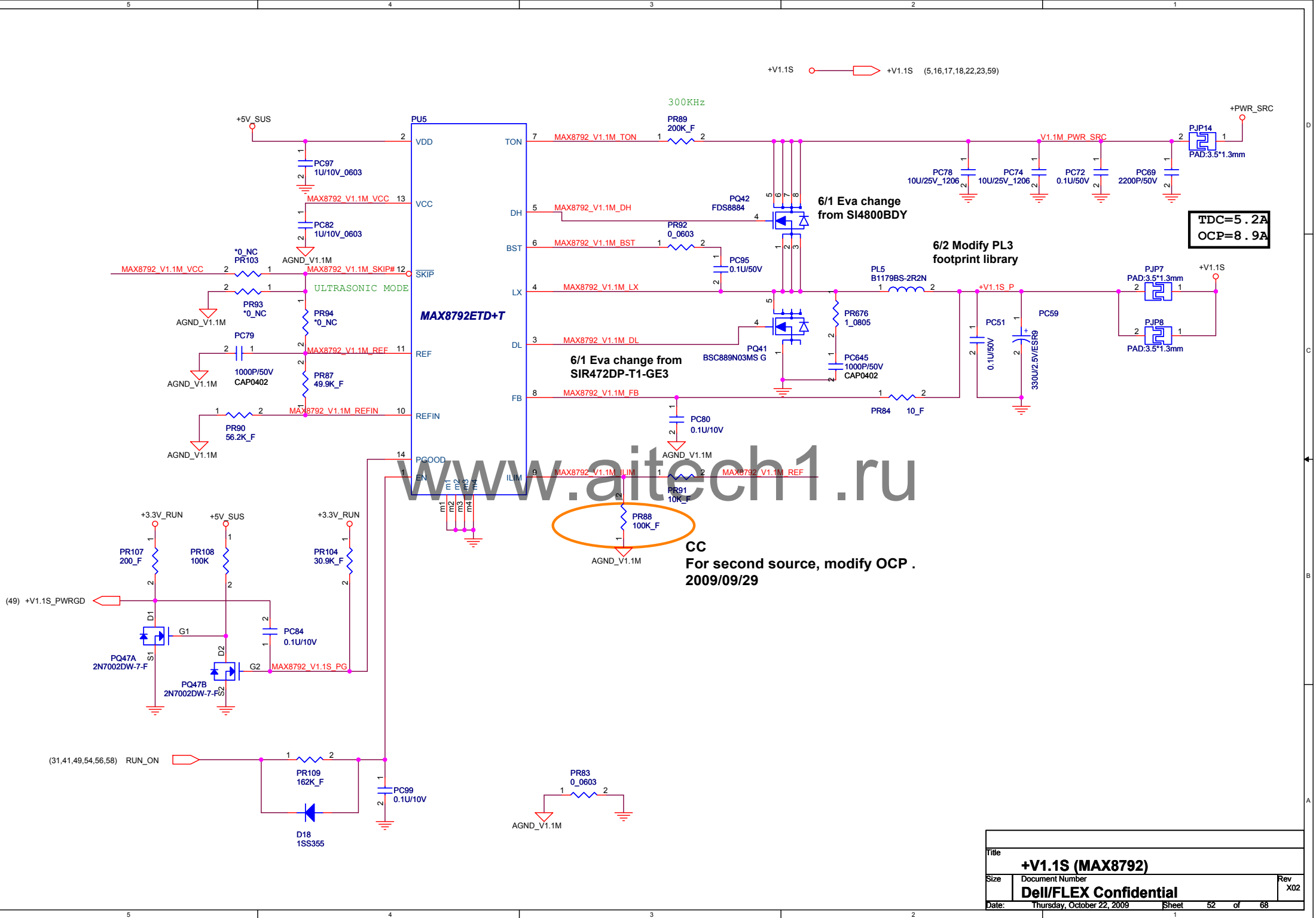
Title			RJ-45/TRANSFORM
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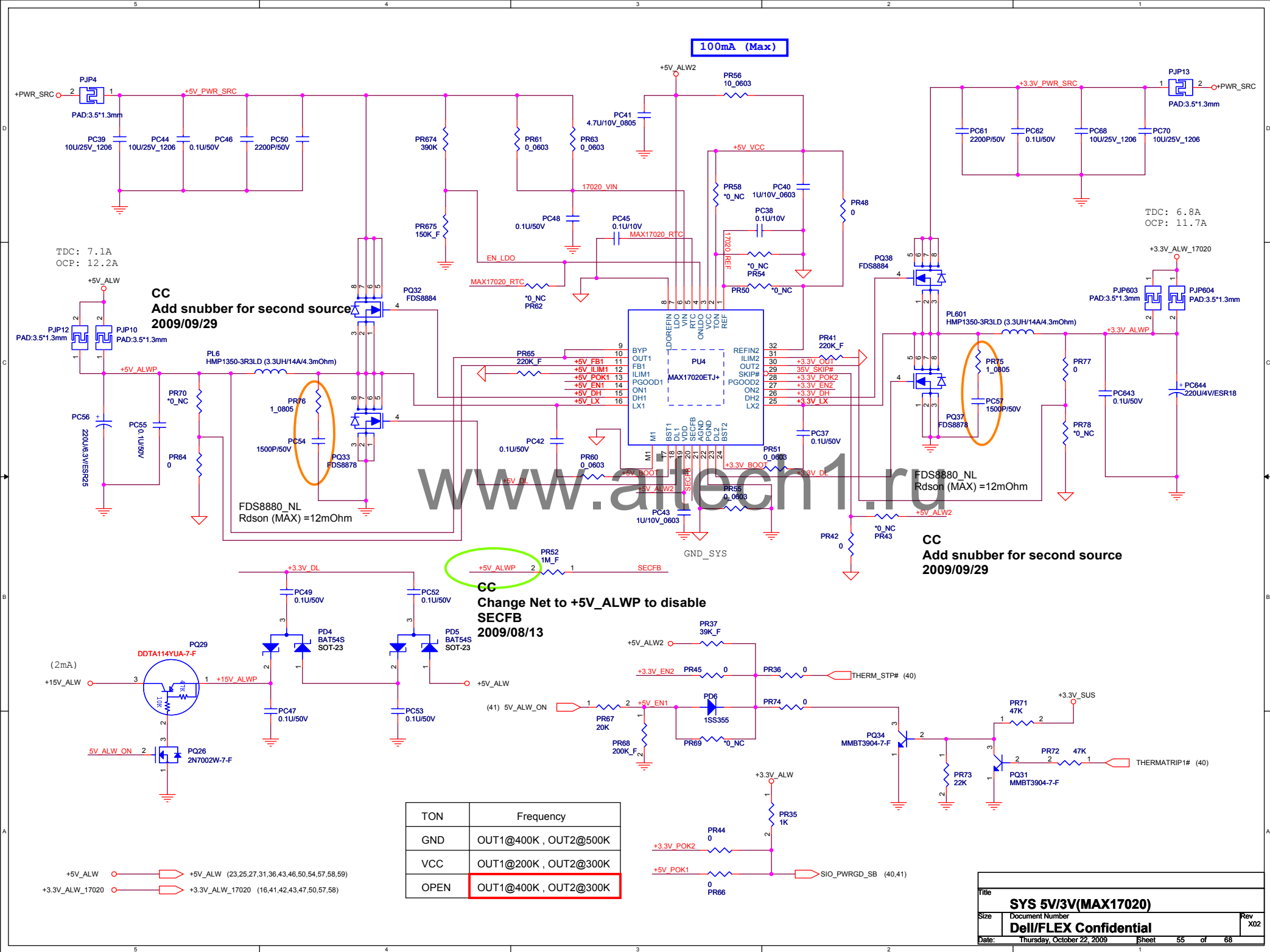


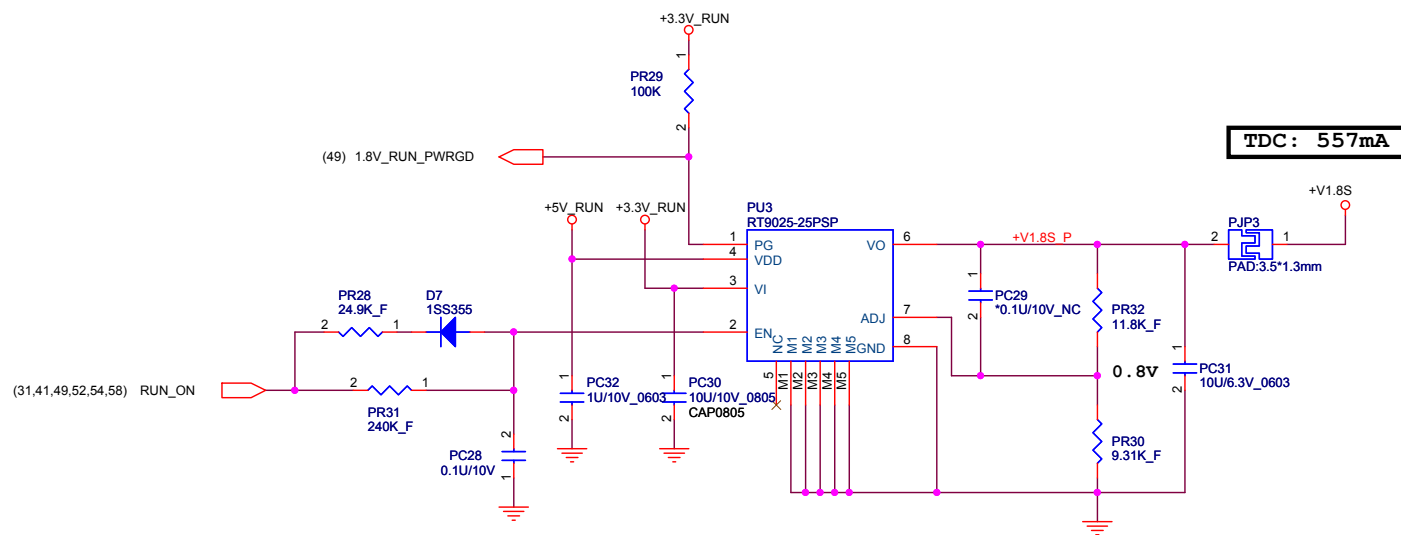
CC
Change to mount such as PU601A, PR609, PR612, PR618...
2009/08/13

File	CPU CORE (MAX17030)		
Size	1000000000		
Doc	Del/FLEX Confidential		
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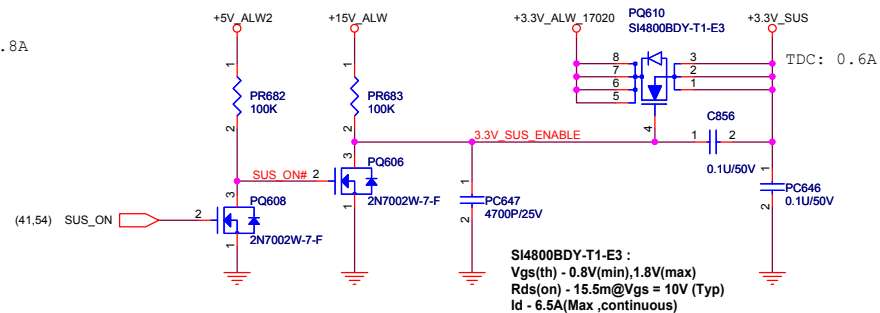
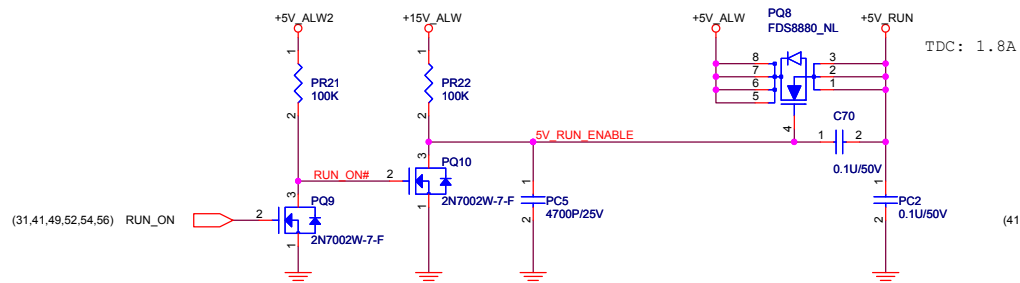
Title			+V1.1S (MAX8792)		
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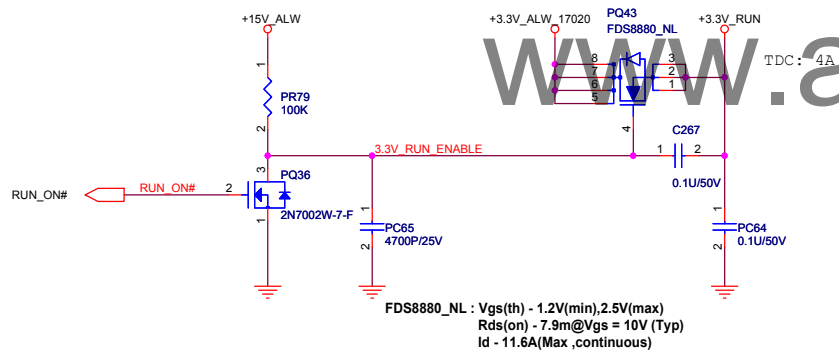
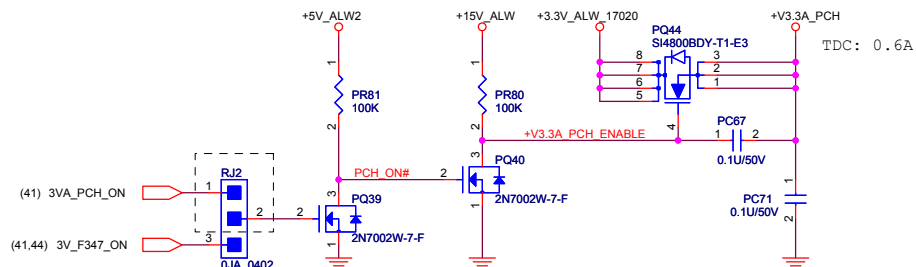
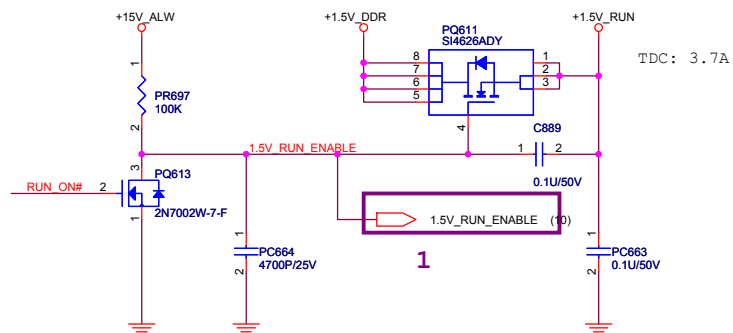


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Title			+V1.8 (RT9025-25PSP)	
Size	Document Number			Rev
	Dell/FLEX Confidential			X02
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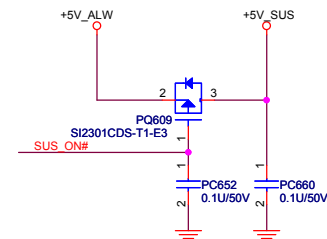
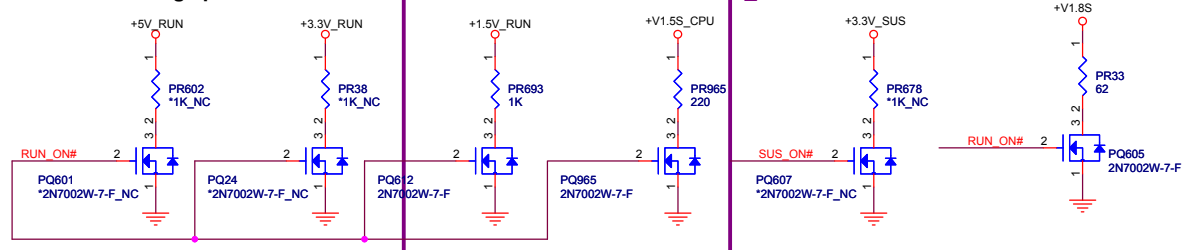


SI4336DY-T1-E3 :
Vgs(th) - 1.0V(min), 3.0V(max)
Rds(on) - 2.6m@Vgs = 10V (Typ)
Id - 17A(Max ,continuous)



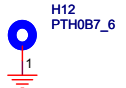
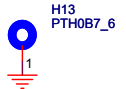
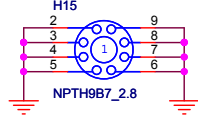
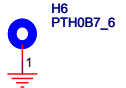
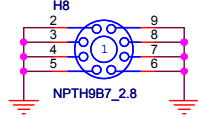
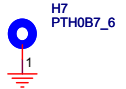
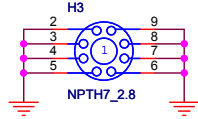
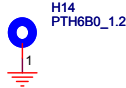
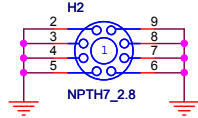
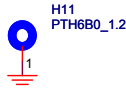
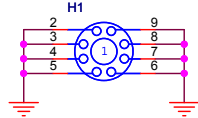
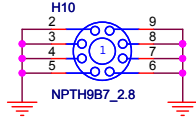
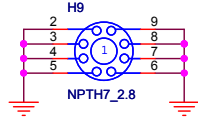
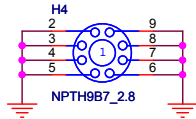
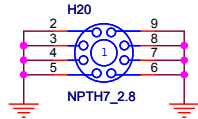
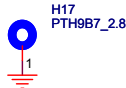
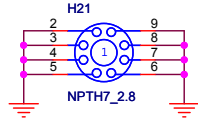
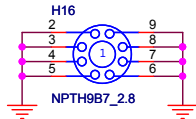
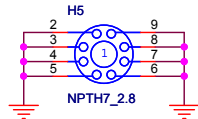
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Reserve discharge path



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RUN POWER SW		
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Screw Hole



FID

FID4
1 NC, NO CONNECT TO ANY.

FID2
1 NC, NO CONNECT TO ANY.

FID3
1 NC, NO CONNECT TO ANY.

FID1
1 NC, NO CONNECT TO ANY.

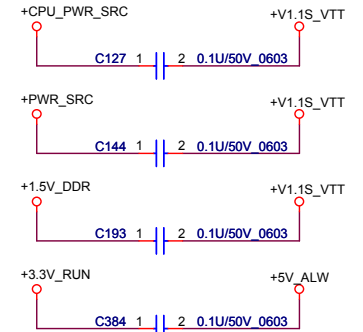
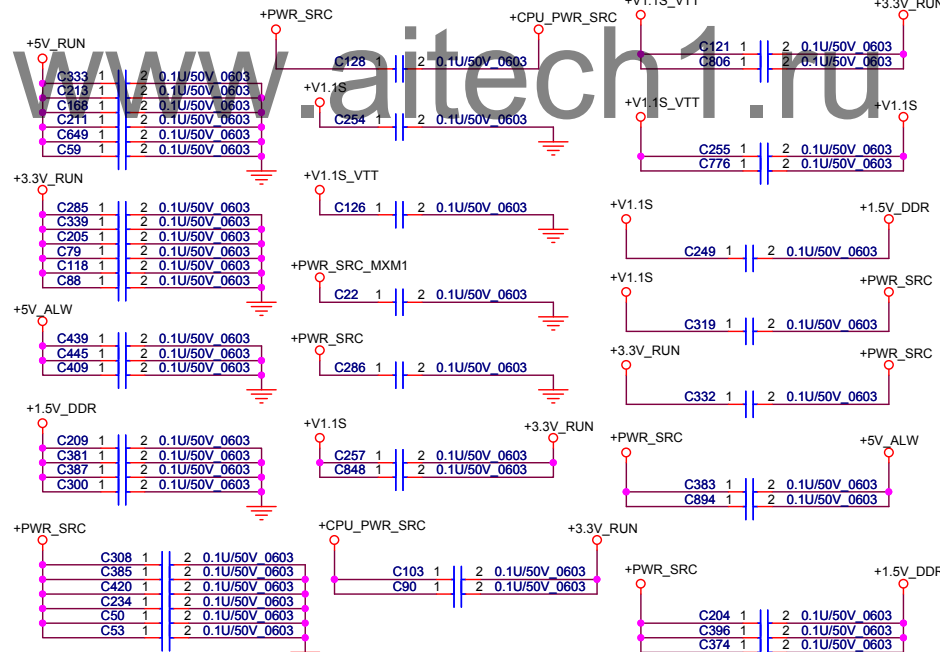
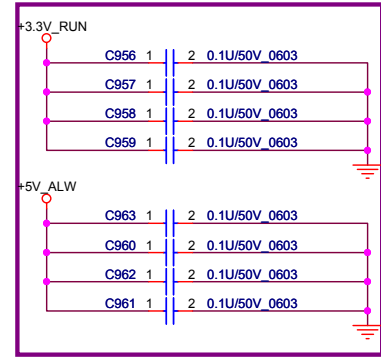
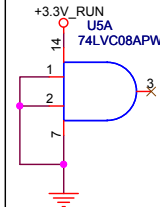
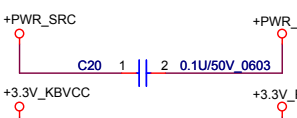
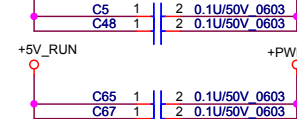
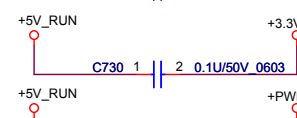
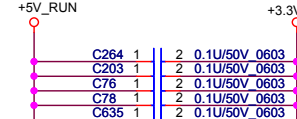
FID604
1 NC, NO CONNECT TO ANY.

FID602
1 NC, NO CONNECT TO ANY.

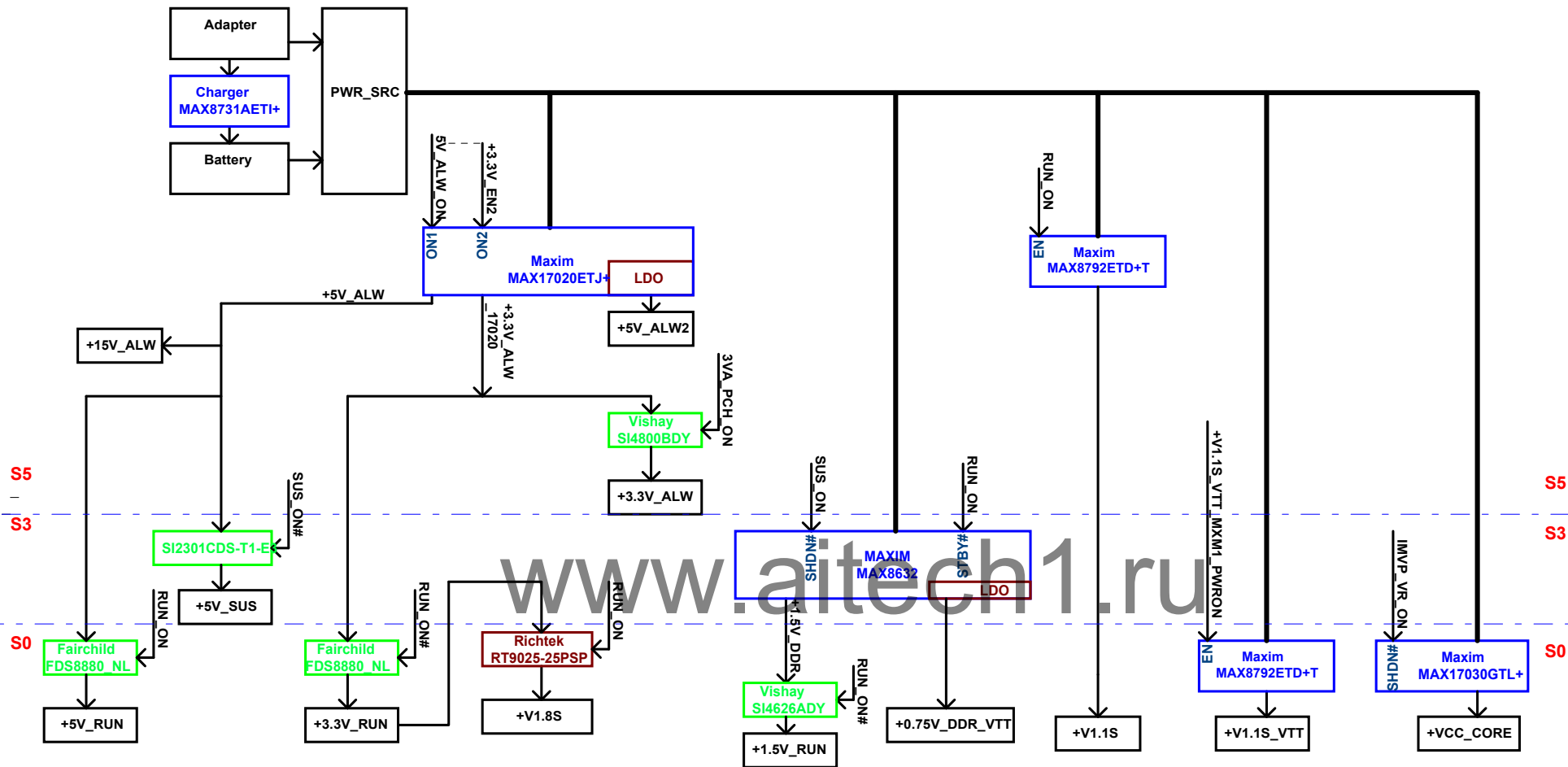
FID603
1 NC, NO CONNECT TO ANY.

FID601
1 NC, NO CONNECT TO ANY.

Moat Cap



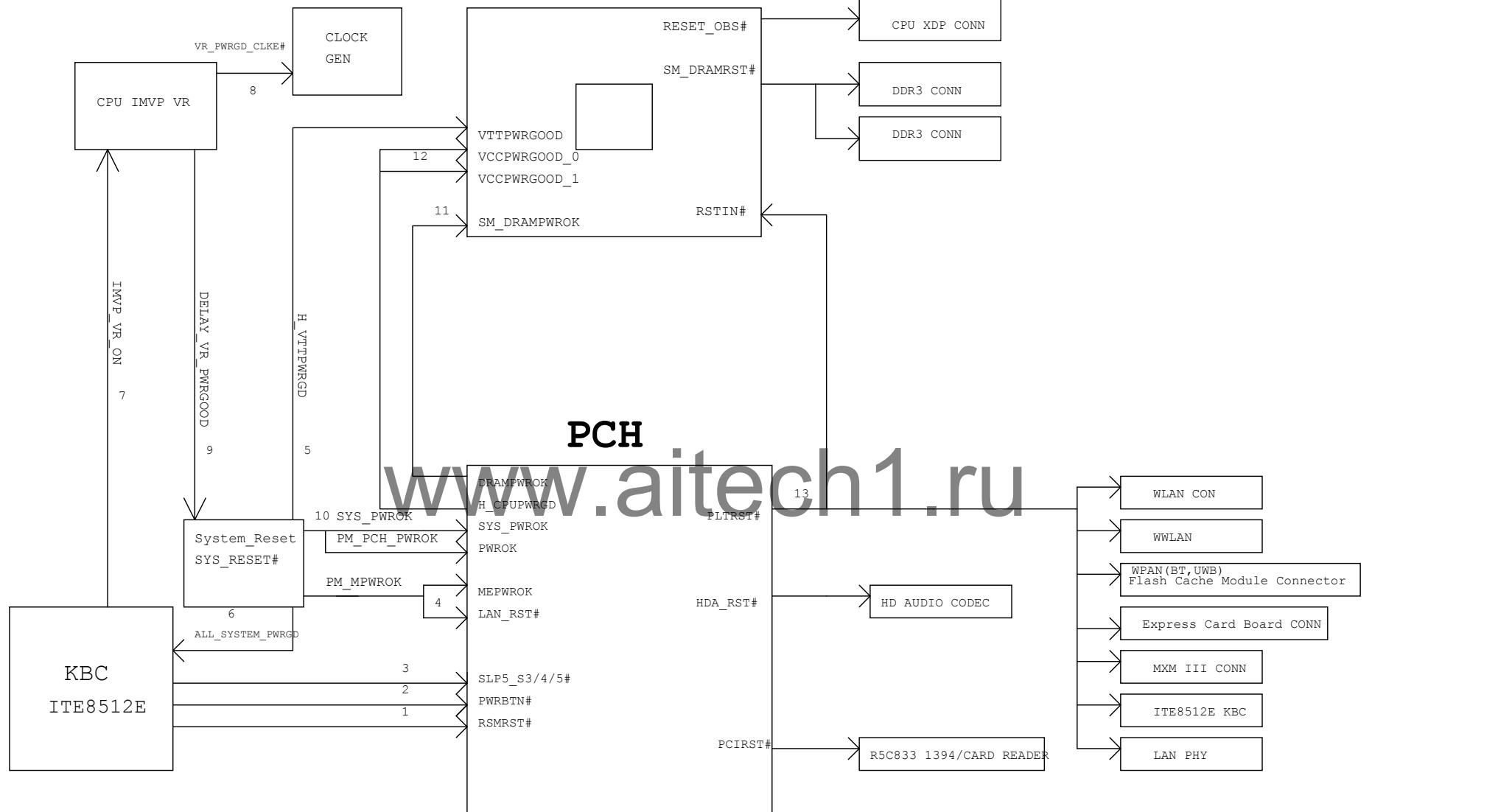
Title			
PAD & SCREW			
Size	Document Number	Rev	
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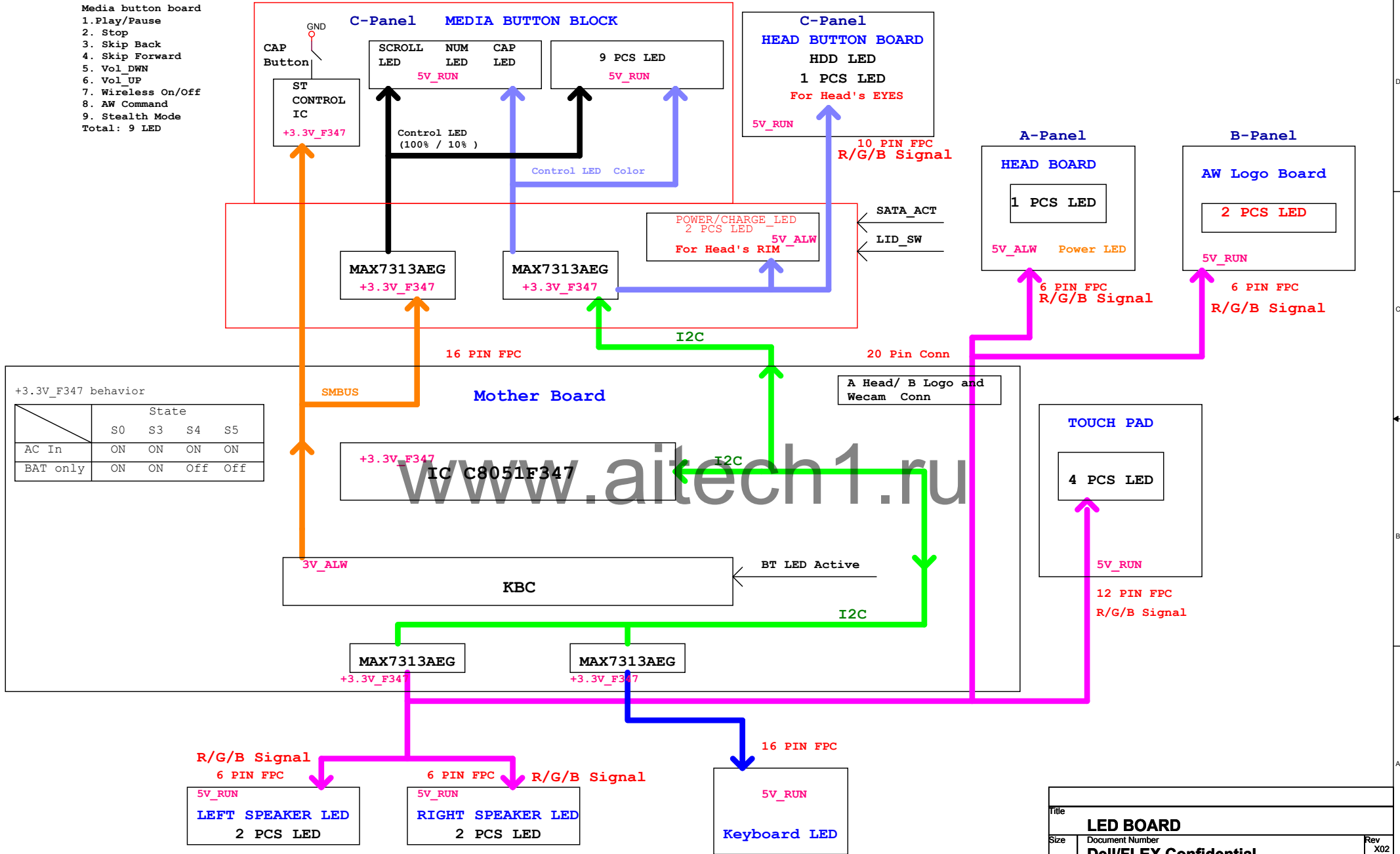
RESET MAP

CPU

PCH



- Media button board
1. Play/Pause
 2. Stop
 3. Skip Back
 4. Skip Forward
 5. Vol_DWN
 6. Vol_UP
 7. Wireless On/Off
 8. AW Command
 9. Stealth Mode
- Total: 9 LED

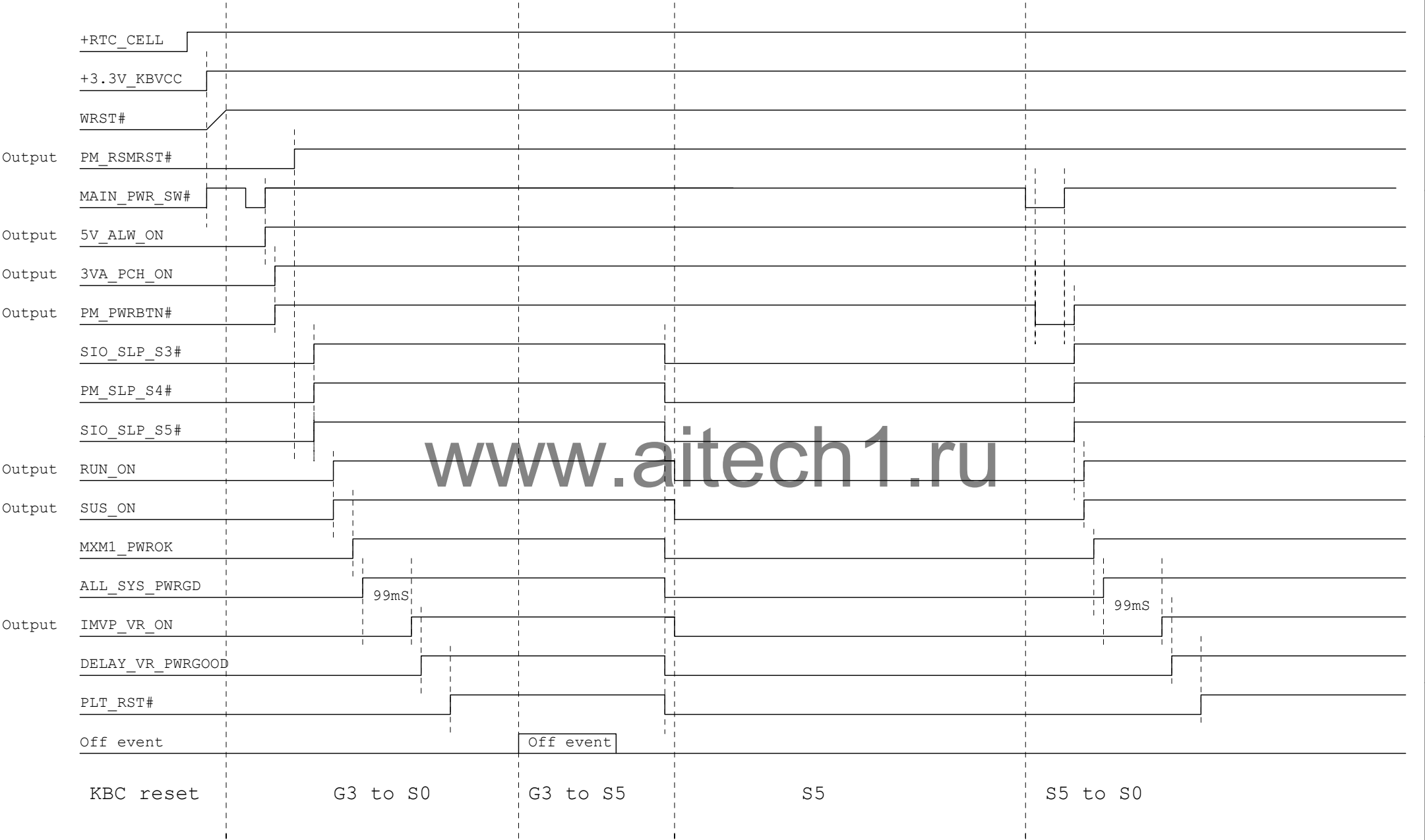


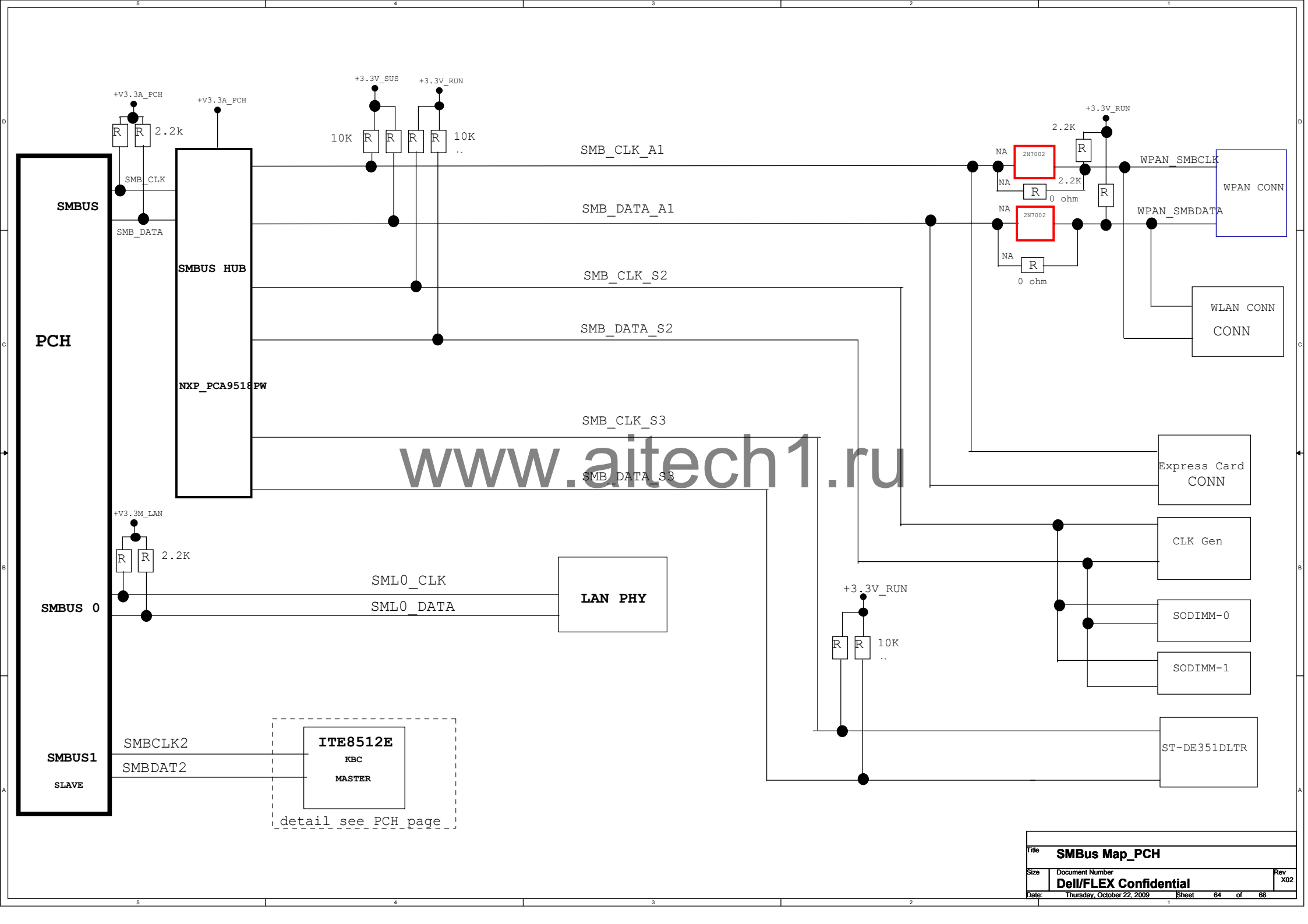
+3.3V_F347 behavior

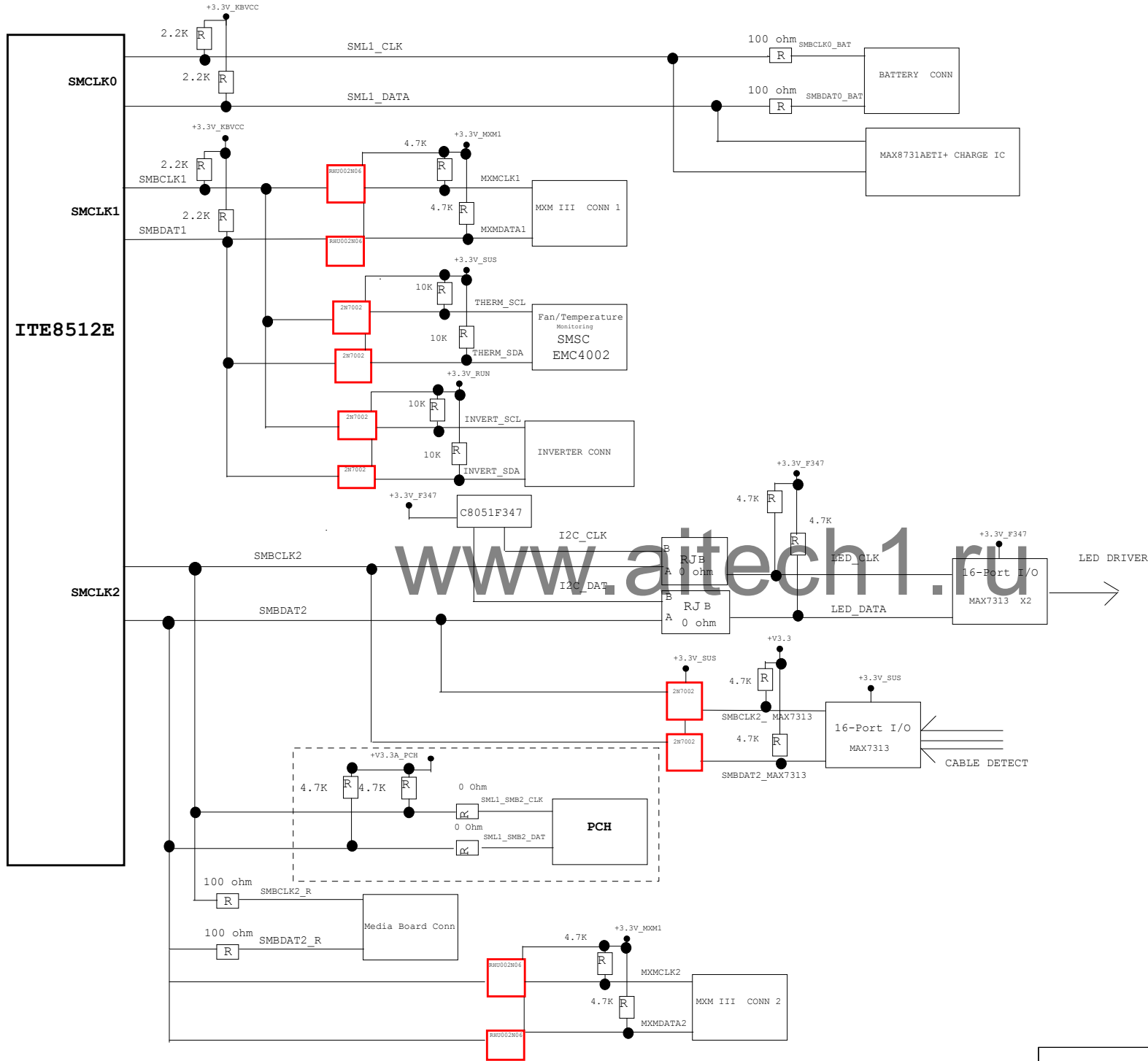
	State			
	S0	S3	S4	S5
AC In	ON	ON	ON	ON
BAT only	ON	ON	Off	Off

Title				
LED BOARD				
Size	Document Number			Rev
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KBC Powre Up Sequence







2009/02/18
1. Add power solution, power link (modify power name +V58 ->+5V_RUN, +V1.55->+1.5V_RUN, +V3.38->+3.3V_RUN, +V3.3->+3.3V_BDS, +V5->+5V_BDS...etc form CPU and Ibox)
2. P.45 Add ONFI connector
3. P.48 Change LAN to SANKEVILLE(R2577)
4. P.1 Modify function block
2009/02/23
1. change EC connect
2. Link USB line
3. Change PCI_QNT#0 to PCI_QNT0#
4. P.24 NVRAM power add a optional 1.8V sch, if ONFI used, using 1.8V
2009/02/24
1. change USB charger component
2. Add some GPIO of PCH for Hybrid
3. modify function block
2009/02/25
1. remove 2 DIMM
2. add EDP connector
3. remove P.50 original power sequence of QS and modify power sequence P.63 than copy to P.50
4. modify LAN chip link p.48
2009/02/26
1. modify the power link from LAN chip to transform and RJ45
2. modify some GPIO pin of P.68
2009/03/04
1. remove HYBRID switchable graphical card schematics
2. remove VGA power of processor and FDI bus for delete VGA support
2009/03/05
1. change SIM slot to WIMAX connector
2009/03/06
1. add PCI-E switch schematics
2009/03/10
1. modify MDM and system power sequence
2. add PM_SLP_S5 ELC to U42
3. p.3. p.4 Description
2009/03/13
1. modify USB nets name from MCM to PCH
2. modify 3904 LIB of P.40
3. add MDM1_PWR0K and MDM2_PWR0K pull high
2009/03/16
1. modify power for placement
2009/03/17
1. modify p. 37, HDD, ODD power controller sch
2. modify MDM_PRESENT to fit Defiant design
3. change to xDR connector to 4 channel
2009/03/19
1. modify p. 23 GPIO
2. modify HPD schematics of HDMI
3. modify p. 15 3/5V power schematics
4. modify p. 56 2.5V feedback resistor
5. add 1.8V dis-charged
2009/03/20
1. modify power p. 51 and p. 57
2. add a reserve pull high resistor at MDM_TRSD
3. complete PCI-E switch schematics
2009/03/23
1. delete P39. R383,R452 and P.38, R380,R416 for dual pull high.
2009/03/24
1. LAN_CLK_REQ#_R with two power source pull high, remove one
2. p. 19 SMBus HUB schematic modify, change mini PCI-E card to separte different power plan with the same channel, and add channel 3 pull high
3. move C1135, C1136, C1138 to p. 64
2009/03/26
1. add G-sensor at p. 37
2. combine +V1.18 and +V1.18_VTT with a power controller
3. add CPU core boost voltage function at p. 52
4. SMB1C2 and SMB1K2 with dual pull high resistor, remove one.
2009/03/30
1. Add jumper between MDM and power
2. remove +3.3V_MDM2 power and modify +3.3V_MDM2 to +3.3V_MDM1
3. CLK_PCH_SRC1_N from A647 of IBEX was wrong, change to CLK_PCH_SRC0_P
4. MDM master, DP HPD_CINX signal remove AND-gate
5. modify MDM_PRESENT# schematic from MDM connector, original with logical gate to 2N7002
2009/04/02
1. remove mini card 3 and SIM card
2. change P07 power plan from run to sus
3. delete p. 60 all most attach cap.
4. integrate TTL logical to reduce the quantity
5. modify +3.3V_ALM to connect to +V3.3A_PCH
2009/06/16
1. modify the schematics to MMD V.3
2009/06/19
1. change the power controller in +V1.18 and +V1.18_VTT to MAX8792
2009/06/20
1. arrange the page number
2. modify the block diagram, frontpage and add smbus map and XBC power up sequence
3. modify the SMBus of Wimax and BT connector as Defiant
2009/06/22
1. modify express card connector definition to differentiate the QS. MLK express card daughter board need to modify. In order to avoid the QS DB enter MLK or MLK DB enter QS, change the pin definition to cut the card reader power.
2. separte MDM2 power
3. change IR power plane to +3.3V_ALM_17020 because of +V3.3A_PCH will be cut when shut down in battery .mode
4. remove TPM and thermal IC un-used part
5. modify U6.18 pin VDD_PWRGD design
6. add second SATA HDD redriver IC
2009/06/30
1. P51 AGNDC net was not connect to system GND, change AGNDC to GND
2. P39 change PCI-E latch connector to SCREW part
3. change U21 pin UDI00 to PCI-E clock request
2009/07/02
1. change U17 part because Capella do not need combine the BIOS into EC flash
2. correct power P0605 schematics
2009/07/06
1. Add SMT stitching CAP
2009/07/08
1. Add CRT DUAL PI filter and by-pass CAP for EMI
2009/07/09
1. reserve IC39LAB3185 co-layout schematics for over-clock function
2. change MDM output configuration to balun

MLK Define	For NV			For AMD	
	N10E-GTX1	N11E-GTX1	N11E-GS1/GE1	M58	Broadway
DPA	HDMI *	HDMI	HDMI	HDMI	HDMI
DPB	No Function	No Function	No Function	No Function	No Function
DPC	No Function	DP *	DP	DP	DP
DPD	No Function	eDP *	eDP	No Function	eDP

2009/07/13
1. modify HDM1_TX*_N and HDM1_TX*_P
2009/07/13
1. rename

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Item	Fix Issue	Reason to change	Rev	Page	Modify list
1 2009/08/4	S3 power reduce	S3 power reduce	X01	7, 10, 12, 21, 49, 54, 58	Intel cut off the +V1.5S CPU power of CPU during S3, therefor , PM_DRAM_FWRGD_R and CPUDRAMRST# need to modify to controller by EC. Follow CRB's suggestion, the controller also need to reserve one from GPIO46 of PCH, original VRDD_1 need to change to GPIO15
2	HDD pin11	add spin-up delay schematic	X01	37	Using FFS_INT2_R of U7 signal to delay HDD spin-up
3 2009/08/5	S3 power reduce	S3 power reduce	X01	12, 41	find GPE1 of EC was not used, take the pin for S3 power reduce item controller
4 2009/08/10	S3 power reduce	Intel's review	X01	58	PR965 change to 220 ohm
5	HDD pin11	reserve the INT2 to PCH	X01	21, 37	add U7 int2 line to PCH's GPIO0 on P37 and P21
6	S3 power reduce	Intel's review	X01	14,15	RJ6 and RJ8 change to mounted B
7	over voltage of VCore	wrong schematics	X01	51	modify PU601.2 connect to PU601.1 directly
8	HDD pin11	wrong schematics	X01	37	modify Q953 and Q954 with wrong direction
9 2009/08/12	ELC controller	LED light on S4	X01	44	add RJ950 for S4 to ELC controller
10	ONFI funtion remove	ONFI was not support	X01	22, 35	un-mounted J3, C448, R857, mounted R858
11	web cam power controller	reserve 7313 20pin	X01	41, 44	CAM_PWR_ON# change to output from U605
12	remove un-used EMI cap	remove un-used EMI cap	X01	48	remove C407, R413, C422, C424, C350, C426, R378
13	VCore overvoltage	X00 stage was not mounted	X01	51	Mounted PU601, PQ603, PQ604, PR606, PR620, PR612, PR618, PC608
14	Intel design guide	change the Cap with low ESR	X01	53	Change the PN of PC34, PC36
15	Power	High side Vds fail	X01	54	Mounted PR141, PC130
16	Power	Change Net to +5V ALWP to enable SECFB	X01	55	Change the +5V ALWP connect to PR52.2
17 2009/08/18	Power	Power fine tune and over voltage schematic's bom change	X01	51, 50,	Change PR679 value to 8.2k, change PR612, PR618 value to 309, mounted PR619, un-mounted PR621
18 2009/08/19	HDD pin11	change INT_2 connect	X01	21	change to GPIO48 of PCH connect to INT_2 of G-sensor
19	MXM2 power control	change the control signal from PCH to EC	X01	21, 41	MXM2_PRESENT#, MXM2_PWR_EN, MXM2_PWROK move to EC, add R973, R971, remove R799, R841
20 2009/08/20	Power	XMP over-voltage solution	X01	54	mounted PR127, Q54, PR129, PR125, Q56, PR134
21	EMI	change the by-pass resistor to choke of USB11	X01	31	un-mounted R43, R42, mounted L4
22	Power	to follow Clarksfield XE load line spec	X01	51	change PR607 to 5.23K
23	BID change to current value	change BID to PT stage	X01	21	mounted R720, un-mounted RT21
24	LAN EA fail issue	modify the layout for LAN routing	X01	48	swap the pin assign of L34, L33 for routing
25	EMI	change the by-pass resistor to choke of USB2	X01	36	un-mounted R433, R434, mounted L38
26 2009/08/22	EMI	Modify RC priority of Media card interface	X01	46	Media card interface from U13 to CN15, original a Cap decoupling then damping a serious resistor change to damping a serious first, then a Cap add.
27 2009/08/25	remove ONFI	remove ONFI	X01	20	un-mounted R284
28	remove EEPROM of media card/1394	change to BIOS confige the controller	X01	46	un-mounted U10, R241. mounted R229
29 2009/08/26	Power	150W power support	X01	50	change PR138 to 10.7k for 150W power support
30	Slave VGA leakage issue	add power split component	X01	27	1. solve RST signal leakage: add a AND gate and R977, R976. 2. ACAV_IN signal leakage: sepearate MXM1 and MXM2, add Q956, R975, Q957 3. CLKREQ signal leakage: add Q958 to cut clkreq if MXM2 power disable. 4. combine THERM_MXM1#, THERM_MXM2# to THERM_MXM#, change GPA5 of EC(original THERM_MXM1#) to MXM_RST.
31 2009/08/27	EMI	add decoupling CAP for EMI	X01	59	+3.3V_RUN add C956, C957, C958, C959, +5V_ALW add C963, C960, C962, C961
32	power leakage	+5V_SUS leakage, change power source of PU6	X01	54	modify PR100 connect to +5V_ALW
33	power leakage	+V3.3M LAN leakage	X01	47	add R981, R980, Q959 to split two power plane
34	power leakage	+3.3V_SUS leakage	X01	41	un-mount R113

Item	Fix Issue	Reason to change	Rev	Page	Modify list
1 2009/09/30	KB LED light uneven	different resistor value of the pin	X02	44	change R748 to 0ohm
2	VCore power	for second source used	X02	51	Change to mount PC16, PC17, PC622, PC19, PC14, PC13 , PR660, PR646, PC636, PC619 for second source
3	charger		X02	50	change PL7, and mounted PR102, PC90
4	modify OCP	modify +V1.1S OCP value	X02	52	change PR88 value
5	3V/5V power	for second source used	X02	55	mounted PR76, PC54, PR75, PC57, change PR41, PR65 value
6	SI measure	add EMI solution will cause SI fail	X02	36	un-mounted L38 and mounted R433, R434
7 2009/10/2	over clock	change over-clock clock GEN	X02	5	change U3 to ICS3185, mounted L16, C139, un-mounted R88, R114
8	remove HDD2 redriver IC	SI could pass without re-driver IC	X02	37	remove C52, C51, C69, C68, U2, C54, C58, C61, C62, R50, R51, R52, R53, R54
9 2009/10/19	tuning the RTC timing	RTC timing will fail in some system in setup menu	X02	16	change C243 to 15pF
10	FDIM test fix	FDIM test fix	X02	9	change C768, C764, C650, C765, C766, C756, C186, C187, C192, C149, C150, C151, C152, C153, C154, C155 to 22uF, change PR634 to 255k ohm, change PC618, PC627, PC616 to 0.22uF/16V, Change PC623, PC617, and PC632 to mount,Change PC635, PC626, PC630, PC631, PC629, PC628 to 470uF/ESR4.5mohm.
11 2009/10/21	MXM2 power leakage	+3.3V_MXM2 with power leakage	X02	27, 28	add D953, D954, D955
12 2009/11/24	LAN LED	LAN LED will light if un-plug LAN and disable LAN function	A00	48	CN19.B1 change to connect to power, and CN19.B2 change to connect to R405.1

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